Li-Ion or Li-Polymer Battery Charger with Low I_q and Accurate Trickle Charge

Check for Samples :bq24741 bq24742

FEATURES

- NMOS-NMOS Synchronous Buck Converter
- Resistor-Programmable Switching Frequency between 300 kHz and 800 kHz
- 9 V-24 V Input Voltage Operation Range
- Support Two to Four Cells
- Analog Inputs with Ratiometric Programming via Resistors or DAC/GPIO
  - Charge Voltage (4-4.512 V/cell)
  - Charge Current (up to 10 A)
  - Adapter Current Limit for DPM
- High-Accuracy Voltage and Current Regulation
  - ±0.5% Charge Voltage Accuracy
  - ±3% Charge Current Accuracy
  - ±3% Adapter Current Accuracy
  - ±2% Input Current Sense Amp Accuracy
- 150 mA Trickle-charge Current with ±33% Accuracy Down to Zero Battery Voltage
- Safety Protection
  - Input Overvoltage Protection
  - Battery Overvoltage Protection
  - Charger Overcurrent Protection
  - Thermal Shutdown Protection
  - FET/Inductor/Battery Short Protection
- Status and Monitoring Outputs
  - Adapter Present Indicator
  - Programmable Input Power Detect with Adjustable Threshold
  - Dynamic Power Management (DPM) with Status Indicator
  - Current Drawn from Input Source
- Charge Enable Pin
- Internal Soft-Start and Loop Compensation
- 25 ns Minimum Driver Dead-Time and 99.5% Maximum Effective Duty Cycle
- 28-pin, 5x5-mm^2 QFN package
- Energy Star Low Quiescent Current I_q
  - < 10 µA Off-State Battery Discharge Current
  - < 1.5 mA Off-State Input Quiescent Current

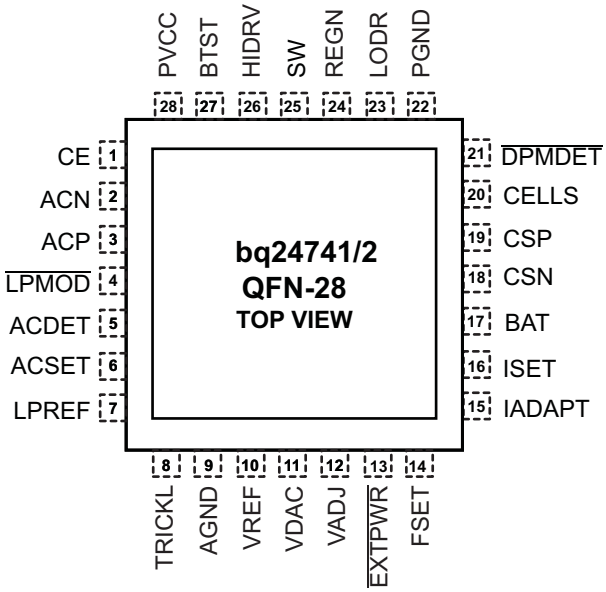
APPLICATIONS

- Notebook and Ultra-Mobile PC
- Portable Data Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Battery Back-up Systems

DESCRIPTION

The bq24741/2 is a high-efficiency, synchronous battery charger with integrated compensation, offering low component count for space-constrained Li-ion or Li-polymer battery charging applications. Ratiometric charge current and voltage programming allows high regulation accuracies, and can be either hardwired with resistors or programmed by the system power-management microcontroller using a DAC or GPIOs.

The bq24741/2 charges two, three, or four series Li+ cells, supporting up to 10 A of charge current, and is available in a 28-pin, 5x5-mm^2 thin QFN package.



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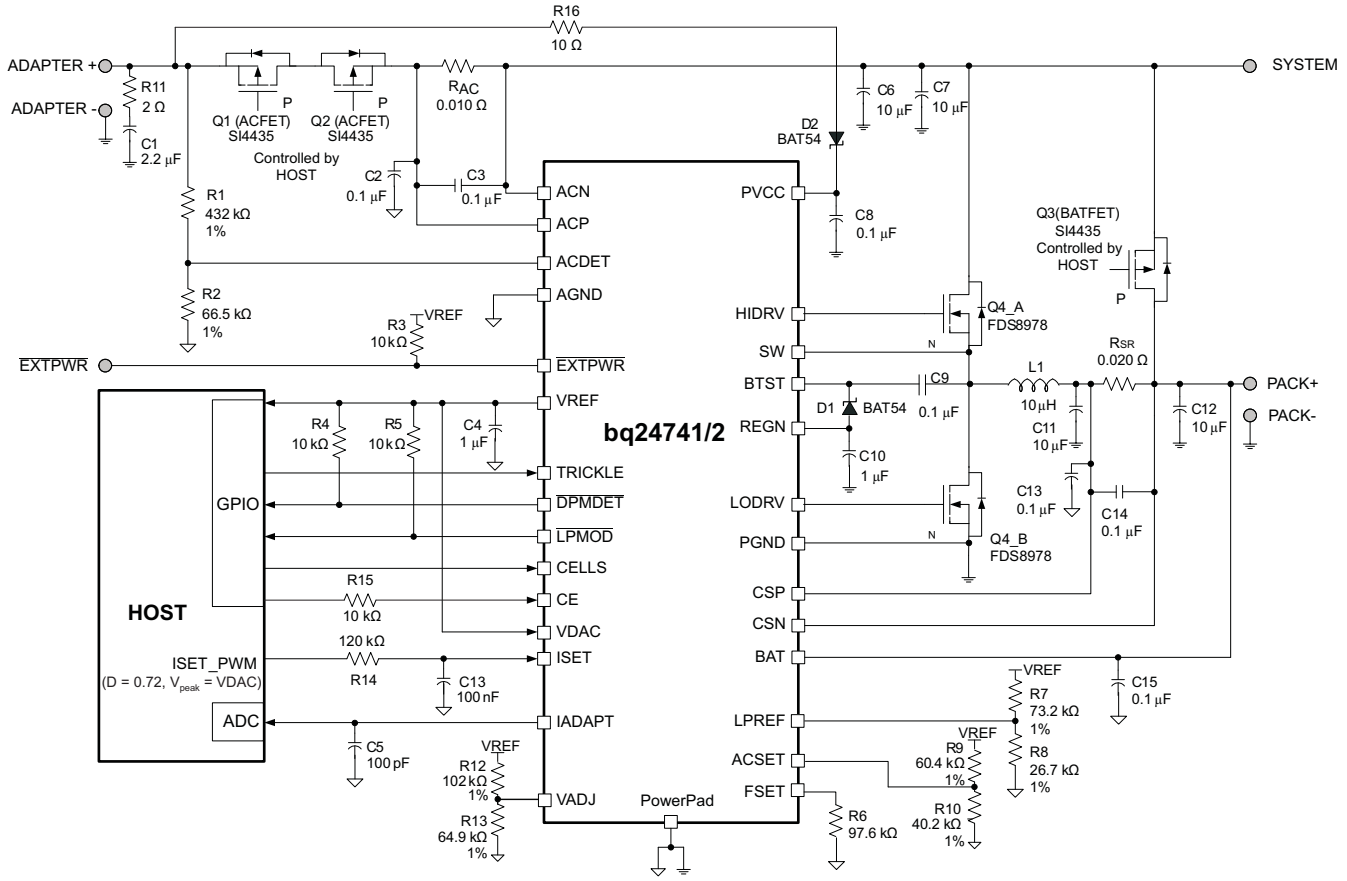
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

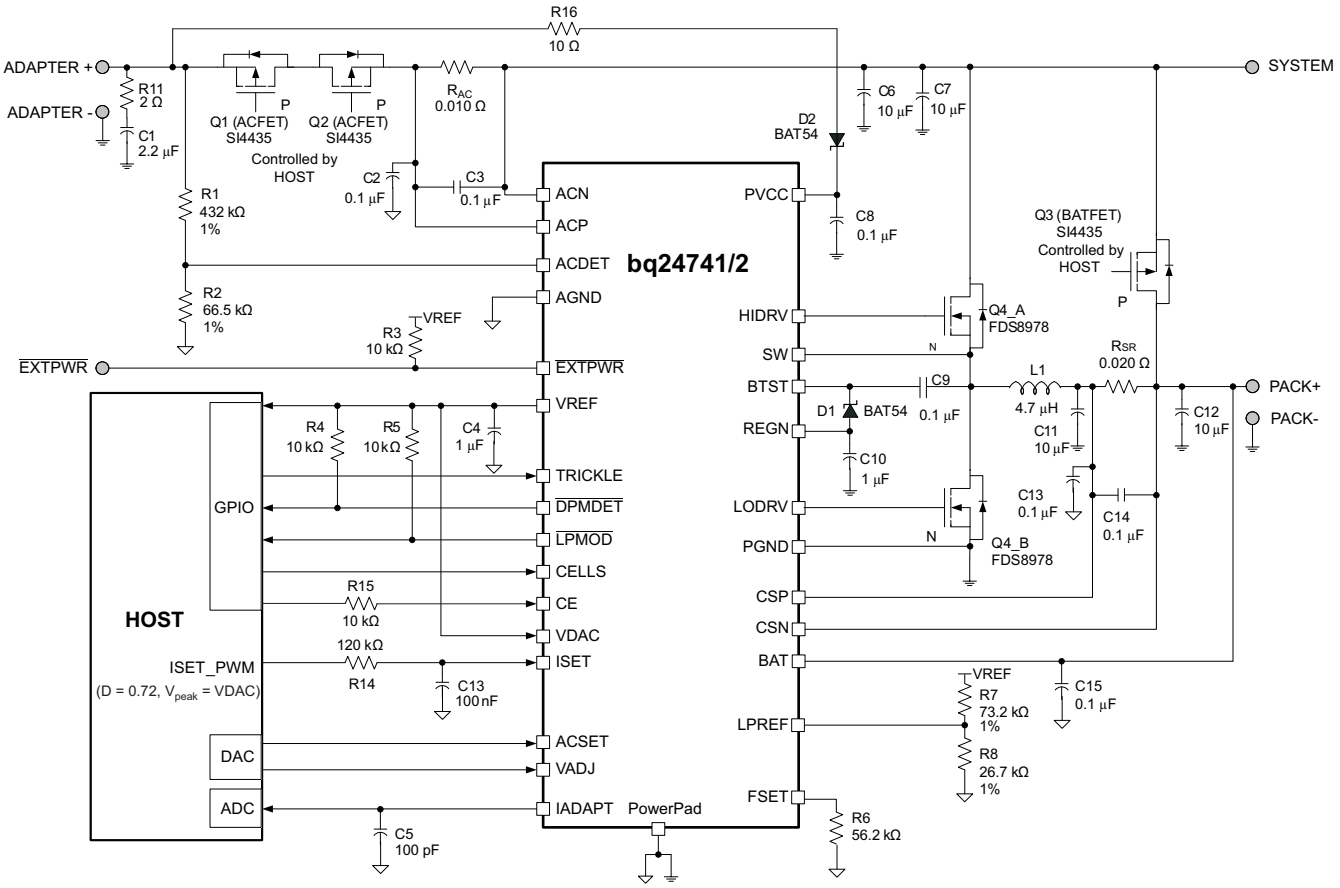
The bq24741/2 features resistor-programmable PWM switching frequency and accurate 150mA trickle charge (with 20 mΩ sensing resistor), which can be enabled via the TRICKLE pin. The bq24741/2 also features Dynamic Power Management (DPM) and input power limiting. These features reduce battery charge current when the input power limit is reached to avoid overloading the AC adapter when supplying the load and the battery charger simultaneously. A high-accuracy current sense amplifier enables accurate measurement of input current from the AC adapter, allowing monitoring the overall system power. If the adapter current is above the programmed low-power threshold, a signal is sent to host so that the system optimizes its power performance according to what is available from the adapter.



F_S = 400 kHz, 90 W Adapter, $V_{ADAPTER}$ = 19 V, V_{BAT} = 3-cell Li-Ion (4.2V/cell), I_{charge} = 3.6 A, $I_{adapter_limit}$ = 4.0 A

Figure 1. Typical System Schematic, Voltage, and Current Programmed by Resistor

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(1) Pull-up rail could be either VREF or other system rail.

(2) SRSET/ACSET could come from either DAC or resistor dividers.

F_S = 650 kHz, 90 W Adapter, $V_{ADAPTER}$ = 19 V, V_{BAT} = 3-cell Li-Ion (4.2V/cell), I_{charge} = 3.6 A, $I_{adapter_limit}$ = 4.0 A

Figure 2. Typical System Schematic, Voltage and Current Programmed by DAC

ORDERING INFORMATION

Part number	Package	Ordering Number (Tape and Reel)	Quantity
bq24741	28-PIN 5 x 5 mm^2 QFN	bq24741RHDR	3000
		bq24741RHDT	250
bq24742	28-PIN 5 x 5 mm^2 QFN	bq24742RHDR	3000
		bq24742RHDT	250

PACKAGE THERMAL DATA

PACKAGE	θ_{JA}	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
QFN – RHD (1) (2)	39°C/W	2.36 W	0.028 W/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2x3 via matrix.

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Table 1. Pin Functions – 28-Pin QFN

PIN		DESCRIPTION
NAME	NO.	
CE	1	Charge-enable active-HIGH logic input. HI enables charge. LO disables charge. It has an internal 1 MΩ pull-down resistor. A 10 KΩ external resistor is required to connect the CE pin to the external pull-up rail other than VREF.
ACN	2	Adapter current sense resistor, negative input. A 0.1 µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1 µF ceramic capacitor is placed from ACN pin to AGND for common-mode filtering.
ACP	3	Adapter current sense resistor, positive input. A 0.1 µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1 µF ceramic capacitor is placed from ACP pin to AGND for common-mode filtering.
$\overline{\text{LPMOD}}$	4	Low-power-mode-detect active-LOW open-drain logic output. Place a 10kohm pull-up resistor from $\overline{\text{LPMOD}}$ pin to the pull-up voltage rail. The output is HI when IADAPT pin voltage is lower than LPREF pin voltage. The output is LOW when IADAPT pin voltage is higher than LPREF pin voltage. Internal 6% hysteresis.
ACDET	5	Adapter detected voltage set input. Program the adapter detect threshold by connecting a resistor divider from adapter input to ACDET pin to AGND pin. Adapter voltage is detected if ACDET pin voltage is greater than 2.4 V. IADAPT current sense amplifier is active when ACDET pin voltage is greater than 0.6V and PVCC > VUVLO. ACOV is input over-voltage protection; it disables charge when ACDET > 3.1 V. ACOV does not latch, and normal operation resumes when ACDET < 3.1 V.
ACSET	6	Adapter current set input. The voltage ratio of ACSET voltage versus VDAC voltage programs the input current regulation set-point during Dynamic Power Management (DPM). Program by connecting a resistor divider from VDAC to ACSET to AGND; or by connecting the output of an external DAC to the ACSET pin and connect the DAC supply to the VDAC pin.
LPREF	7	Low power voltage set input. Connect a resistor divider from VREF to LPREF, and AGND to program the reference for the LOPWR comparator. The LPREF pin voltage is compared to the IADAPT pin voltage and the logic output is given on the $\overline{\text{LPMOD}}$ open-drain pin. Connect LPREF to ACSET through a resistor divider to track the adapter power.
TRICKLE	8	Trickle current enable logic input. When CE is HIGH, a HIGH level on this pin enables accurate 150 mA trickle charge with 20 mΩ sense resistor. A LOW level on this pin enables the ISET pin to program the charge current. It has an internal 1MΩ pull-down resistor.
AGND	9	Analog ground. Ground connection for low-current sensitive analog and digital signals. On PCB layout, connect to the analog ground plane, and only connect to PGND through the PowerPad underneath the IC.
VREF	10	3.3 V regulated voltage output. Place a 1 µF ceramic capacitor from VREF to AGND pin close to the IC. This voltage could be used for ratio-metric programming of voltage and current regulation and for programming the LPREF threshold. VREF is also the voltage source for the internal circuit.
VDAC	11	Charge voltage set reference input. Connect the VREF or external DAC voltage source to VDAC pin. Battery voltage, charge current, and input current are programmed as a ratio of the VDAC pin voltage versus the voltage on VADJ, and ACSET pin voltages, respectively. Place resistor dividers from VDAC to VADJ, ISET, and ACSET pins to AGND for programming. A DAC could be used by connecting the DAC supply to VDAC and connecting the output to VADJ, ISET, or ACSET.
VADJ	12	Charge voltage set input. The voltage ratio of VADJ voltage versus VDAC voltage programs the battery voltage regulation set-point. Program by connecting a resistor divider from VDAC to VADJ, to AGND; or, by connecting the output of an external DAC to VADJ pin and connect the DAC supply to VDAC pin.
$\overline{\text{EXTPWR}}$	13	Valid adapter active-low detect logic open-drain output. Pulled LO when Input voltage is above ACDET programmed threshold OR input current is greater than 1.25 A with 10 mΩ sense resistor. Connect a 10 kΩ pull-up resistor from $\overline{\text{EXTPWR}}$ pin to pull-up supply rail.
FSET	14	PWM switching frequency (F_S) program pin. Program the switching frequency by placing a resistor to AGND on this pin.
IADAPT	15	Adapter current sense amplifier output. IADAPT voltage is 20 times the differential voltage across ACP-ACN. Place a 100pF (max) or less ceramic decoupling capacitor from IADAPT to AGND.
ISET	16	Charge current set input. The voltage ratio of ISET voltage versus VDAC voltage programs the charge current regulation set-point. Program by connecting a resistor divider from VDAC to ISET, to AGND; or, by connecting the output of an external DAC to ISET pin and connect the DAC supply to VDAC pin.
BAT	17	Battery voltage remote sense. Directly connect a kelvin sense trace from the battery pack positive terminal to the BAT pin to accurately sense the battery pack voltage. Place a 0.1 µF capacitor from BAT to AGND close to the IC to filter high frequency noise.
CSN	18	Charge current sense resistor, negative input. A 0.1 µF ceramic capacitor is placed from CSN to CSP to provide differential-mode filtering. An optional 0.1 µF ceramic capacitor is placed from CSN pin to AGND for common-mode filtering.
CSP	19	Charge current sense resistor, positive input. A 0.1 µF ceramic capacitor is placed from CSN to CSP to provide differential-mode filtering. A 0.1 µF ceramic capacitor is placed from CSP pin to AGND for common-mode filtering.
CELLS	20	2, 3 or 4 cells selection logic input. Logic Lo programs 3–cell. Logic HI programs 4-cell. Floating programs 2–cell.

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Table 1. Pin Functions – 28-Pin QFN (continued)

PIN		DESCRIPTION
NAME	NO.	
$\overline{\text{DPMDET}}$	21	Dynamic power management (DPM) input current loop active, open-drain output status. Logic low (LO) indicates input current is being limited by reducing the charge current. Connect 10-kohm pull-up resistor from $\overline{\text{DPMDET}}$ pin to VREF or a different pull-up supply rail.
PGND	22	Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to source of low-side power MOSFET, to ground connection of in put and output capacitors of the charger. Only connect to AGND through the PowerPad underneath the IC.
LODRV	23	PWM low side driver output. Connect to the gate of the low–side power MOSFET with a short and wide trace.
REGN	24	PWM low side driver positive supply output. Connect a 1 µF ceramic capacitor from REGN to PGND pin, close to the IC. Use for low side driver and high-side driver bootstrap voltage by connecting a small signal Schottky diode from REGN to BTST. REGN is disabled when CE is LOW.
SW	25	PWM high side driver negative supply. Connect to the Phase switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1 µF bootstrap capacitor from SW to BTST.
HIDRV	26	PWM high side driver output. Connect to the gate of the high-side power MOSFET with a short trace.
BTST	27	PWM high side driver positive supply. Connect a 0.1 µF bootstrap ceramic capacitor from BTST to SW. Connect a bootstrap Schottky diode from REGN to BTST. A optional 2.0Ω - 5.1Ω bootstrap resistor can be inserted between the BTST pin and the common point of the bootstrap capacitor and bootstrap diode, thus dampening the SW node voltage ring and spike.
PVCC	28	IC power positive supply. Connect to the adapter input through a schottky diode. Place a 0.1 uF ceramic capacitor from PVCC to PGND pin close to the IC.
PowerPad		Exposed pad beneath the IC. AGND and PGND star-connected only at the PowerPad plane. Always solder PowerPad to the board, and have vias on the PowerPad plane connecting to AGND and PGND planes. It also serves as a thermal pad to dissipate the heat.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
Voltage range	PVCC, ACP, ACN, CSP, CSN, BAT	–0.3 to 30	V
	SW	–1 to 30	
	REGN, LODRV, VADJ, ACSET, ISET, ACDET, FSET, IADAPT, $\overline{\text{LPMOD}}$, LPREF, CE, CELLS, $\overline{\text{EXTPWR}}$, $\overline{\text{DPMDET}}$, TRICKLE	–0.3 to 7	
	VDAC, VREF	–0.3 to 3.6	
	BTST, HIDRV with respect to AGND and PGND	–0.3 to 36	
	AGND, PGND	–1 to 1	
Maximum difference voltage	ACP–ACN, CSP–CSN	-0.5 to 0.5	
Junction temperature range		–40 to 155	°C
Storage temperature range		–55 to 155	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage range	SW	–0.8		24	V
	PVCC, ACP, ACN, CSP, CSN, BAT	0		24	V
	REGN, LODRV	0		6.5	V
	VREF		3.3		V
	VDAC		3.6		V
	VADJ, ACSET, ISET, ACDET, FSET, IADAPT, $\overline{\text{LPMOD}}$, LPREF, CE, CELLS, $\overline{\text{EXTPWR}}$, $\overline{\text{DPMDET}}$, TRICKLE	0		5.5	V
	BTST, HIDRV with respect to AGND and PGND	0		30	V
	AGND, PGND	–0.3		0.3	V
Maximum difference voltage: ACP–ACN, CSP–CSN		–0.3		0.3	V
Junction temperature range		–40		125	°C
Storage temperature range		–55		150	°C

ELECTRICAL CHARACTERISTICS

9.0 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, F_s=600 kHz, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted) (1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{PVCC_OP}	PVCC input voltage operating range		9		24	V
CHARGE VOLTAGE REGULATION						
$V_{BAT_REG_RNG}$	BAT voltage regulation range	4-4.512 V per cell, times 2,3,4 cells	8		18.048	V
V_{VDAC_OP}	VDAC reference voltage range		2.6		3.6	V
V_{VADJ_OP}	VADJ voltage range		0		VDAC	V
	Charge voltage regulation accuracy	8 V, 8.4 V, 9.024 V	–0.5		0.5	%
		12 V, 12.6 V, 13.536 V	–0.5		0.5	
		16 V, 16.8 V, 18.048 V	–0.5		0.5	
CHARGE CURRENT REGULATION (ENABLE CE & DISABLE TRICKLE)						
V_{IREG_CHG}	Charge current regulation differential voltage range	$V_{IREG_CHG} = V_{CSP} – V_{CSN}$	0		100	mV
V_{ISET_OP}	SRSET voltage range		0		VDAC	V
	Charge current regulation accuracy	V_{IREG_CHG} = 40 mV	–3%		3%	
		V_{IREG_CHG} = 20 mV	–5%		5%	
		V_{IREG_CHG} = 5 mV	–25%		25%	
		V_{IREG_CHG} = 3 mV (V_{BAT} ≥ 4 V)	–33%		33%	
		V_{IREG_CHG} = 3 mV (V_{BAT} < 4 V)	–50%		50%	
	Off-set Voltage of Amplifier	V_{BAT} ≥ 4 V	–1.0		1.0	mV
		V_{BAT} < 4 V	–1.5		1.5	
TRICKLE CHARGE CURRENT REGULATION (ENABLE CE & TRICKLE)						
	Charge Current Regulation Accuracy	V_{IREG_CHG} = 3 mV	–33%		33%	
	Off-set Voltage of Amplifier		–1.0		1.0	mV

(1) Verified by design
(2) Deglitch time and delay are proportional to the period of oscillator, unless specified.
(3) When CE=HIGH, the internal oscillator frequency is equal to external setting F_s; when CE=LOW, the internal oscillator frequency is fixed internal setting 700 kHz.

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ELECTRICAL CHARACTERISTICS (continued)

9.0 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, F_s=600 kHz, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted) (1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT REGULATION						
V_{IREG_DPM}	Adapter current regulation differential voltage range	$V_{IREG_DPM} = V_{ACP} – V_{ACN}$	0		100	mV
V_{ACSET_OP}	ACSET voltage range		0		VDAC	V
	Input current regulation accuracy	V_{IREG_DPM} = 40 mV	–3%		3%	
		V_{IREG_DPM} = 20 mV	–5%		5%	
		V_{IREG_DPM} = 5 mV	–25%		25%	
		V_{IREG_DPM} = 1.5 mV	–33%		33%	
	Off-set Voltage of Amplifier		-500		500	µV
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	V_{ACDET} > 0.6 V, 0-30 mA	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF short current limit	V_{VREF} = 0 V, V_{ACDET} > 0.6 V	35		80	mA
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{ACDET} > 0.6 V, 0-75 mA, PVCC > 10 V	5.6	5.9	6.2	V
I_{REGN_LIM}	REGN short current limit	V_{REGN} = 0 V, V_{ACDET} > 0.6 V	90		145	mA
ADAPTER CURRENT SENSE AMPLIFIER						
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/ACN	0		24	V
V_{IADAPT}	IADAPT output voltage range		0		2	
I_{IADAPT}	IADAPT output current		0		1	mA
A_{IADAPT}	Current sense amplifier voltage gain	$A_{IADAPT} = V_{IADAPT} / V_{IREG_DPM}$		20		V/V
	Adapter current sense accuracy	V_{IREG_DPM} = 40 mV	–2%		2%	
		V_{IREG_DPM} = 20 mV	–4%		4%	
		V_{IREG_DPM} = 5 mV	–25%		25%	
		V_{IREG_DPM} = 1.5 mV	–33%		33%	
I_{IADAPT_LIM}	Output short current limit	V_{IADAPT} = 0 V	1			mA
C_{IADAPT_MAX}	Maximum output load capacitance	For stability with 0 mA to 1 mA load			100	pF
ACDET COMPARATOR (INPUT UNDER_VOLTAGE, ACVGOOD)						
V_{ACDET_CHG}	ACDET adapter-detect rising threshold	Min voltage to enable charging, V_{ACDET} rising	2.376	2.40	2.424	V
$V_{ACDET_CHG_HYS}$	ACDET falling hysteresis	V_{ACDET} falling, PVCC>8V		40		mV
	ACDET rising deglitch to turn on $\overline{\text{EXTPWR}}$ FET(4)	V_{ACDET} rising, PVCC>8V		1.2		ms
	ACDET rising deglitch to enable charge (4)	V_{ACDET} rising, PVCC>8V, CE=HIGH		333		ms
	ACDET falling deglitch to turn off $\overline{\text{EXTPWR}}$ FET(4)	V_{ACDET} falling, PVCC>8V		80		µs
	ACDET falling deglitch to disable charge(4)	V_{ACDET} falling, PVCC>8V		80		µs
$T_{ACDET_\overline{EXTPWR}}$	Power-up delay from V_{ACDET}>2.4V to $\overline{\text{EXTPWR}}$ FET turn-on(4)	First time power up, F_s = 300 kHz – 800 kHz			2	ms
AC CURRENT DETECT COMPARATOR (INPUT UNDER_CURRENT, ACIGOOD)						
V_{ACIDET}	Adapter current detect falling threshold	V_{ACI} = 20 X I_{AC} x R_{AC}, falling edge	200	250	300	mV
V_{ACIDE_HYS}	Adapter current detect hysteresis	Rising edge		50		mV
	Adapter current detect deglitch	IADAPT rising		10		µs
		IADAPT falling		10		µs

(4) Verified by design

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ELECTRICAL CHARACTERISTICS (continued)

9.0 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, F_s=600 kHz, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted) (1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PVCC / BAT COMPARATOR						
$V_{PVCC_BAT_OP}$	Differential Voltage from PVCC to BAT		-20		24	V
$V_{PVCC-BAT_FALL}$	PVCC to BAT falling threshold	V_{PVCC} – V_{BAT} to disable charge	850	900	950	mV
$V_{PVCC-BAT_HYS}$	PVCC to BAT hysteresis		200	225	250	mV
	PVCC to BAT rising deglitch	V_{PVCC} – V_{BAT} > $V_{PVCC-BAT_RISE}$		4.5		ms
	PVCC to BAT falling deglitch	V_{PVCC} – V_{BAT} < $V_{PVCC-BAT_FALL}$		10		µs
BAT OVERVOLTAGE COMPARATOR						
V_{OV_RISE}	Overvoltage rising threshold(5)	As percentage of V_{BAT_REG}		104%		
V_{OV_FALL}	Overvoltage falling threshold(5)	As percentage of V_{BAT_REG}		102%		
BATSHORT COMPARATOR						
$V_{BATSHORT_RISE}$	Battery rising voltage for BATSHORT exit			2		V/Cell
$V_{BATSHORT_FALL}$	Battery falling voltage for BATSHORT entry			1.7		V/Cell
CHARGE OVERCURRENT COMPARATOR						
V_{OC_peak}	Peak charge over-current threshold	$V_{(CSP-\ CSN)}$, when V_{ISET} / VDAC < 0.8	90	110	130	mV
		$V_{(CSP-\ CSN)}$, when V_{ISET} / V_{DAC} ≥ 0.8	100	125	150	mV
MOSFET SHORT PROTECTION COMPARATOR						
V_{HS}	High-side Threshold (bq24741)	Measured on ACP-SW	120	250	455	mV
V_{HS}	High-side Threshold (bq24742)	Measured on ACP-SW	475	750	1065	mV
V_{LS}	Low-side Threshold	Measured on SW-AGND	90	160	320	mV
CHARGE UNDERCURRENT PROTECTION COMPARATOR (UCP)						
V_{UCP}	Charge under-current threshold, falling edge	$V_{(CSP-\ CSN)}$ from synchronous to non-synchronous operation	25	30	35	mV
	Charge under-current threshold, rising edge	$V_{(CSP-CSN)}$ from non-synchronous to synchronous operation	35	40	45	mV
	Charge under-current rising deglitch			10		µs
	Charge under-current falling deglitch			320		µs
INPUT OVERVOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC over-voltage rising threshold on ACDET	Measure on ACDET pin	3.007	3.1	3.193	V
V_{ACOV_HYS}	AC over-voltage deglitch (rising edge)			650		µs
	AC over-voltage deglitch (falling edge)			650		µs
INPUT UNDERVOLTAGE LOCK-OUT COMPARATOR (UVLO)						
V_{UVLO}	AC under-voltage rising threshold	Measured on PVCC pin	7	8	9	V
V_{UVLO_HYS}	AC under-voltage hysteresis			260		mV
INPUT LOW POWER MODE COMPARATOR ($\overline{LPMOD}$)						
V_{ACLP_HYS}	AC low power mode comparator internal hysteresis		5%		7%	
V_{ACLP_OFFSET}	AC low power mode comparator offset voltage			1		mV
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature Increasing		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling			20		°C
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS_HI_ON}$	High side driver turn-on resistance	V_{BTST} – V_{SW} = 5.5 V, tested at 100 mA			6	Ω
$R_{DS_HI_OFF}$	High side driver turn-off resistance	V_{BTST} – V_{SW} = 5.5 V, tested at 100 mA			1.4	Ω
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold voltage	V_{BTST} – V_{SW} when low side refresh pulse is requested	4			V
I_{BTST_LEAK}	BTST leakage current	High side is on; charge enabled			200	µA

(5) Verified by design

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ELECTRICAL CHARACTERISTICS (continued)

9.0 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, F_s=600 kHz, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted) (1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS_LO_ON}$	Low side driver turn-on resistance	REGN = 6 V, tested at 100 mA			6	Ω
$R_{DS_LO_OFF}$	Low side driver turn-off resistance	REGN = 6 V, tested at 100 mA			1.2	Ω
PWM DRIVERS TIMING						
	Driver Dead Time between HIDRV and LODRV		25			ns
PWM OSCILLATOR						
F_S	Programmable PWM switching frequency range	R_{FSET}=130 kΩ - 45 kΩ	300		800	kHz
	PWM switching frequency accuracy		-20%		20%	
	RAMP amplitude			1.33		V
	DC offset of RAMP			300		mV
QUIESCENT CURRENT						
I_{OFF_STATE}	Total off-state quiescent current into pins: CSP, CSN, BAT, BTST, SW, PVCC, ACP, ACN	V_{BAT} = 16.8 V, V_{ACDET} < 0.6 V, V_{PVCC} > 8 V, T_J = 0 to 125°C		7	11	µA
	Total off-state battery current from ACP, ACN	V_{BAT} = 16.8 V, V_{ACDET} < 0.6 V, V_{PVCC} > 8 V, T_J = 0 to 125°C			1	µA
I_{BAT_ON}	Battery on-state quiescent current	V_{BAT} = 16.8 , 0.6 V < V_{ACDET} < 2.4 V, V_{PVCC} > 8V		1		mA
I_{BATQ_CD}	Total quiescent current into CSP, CSN, BAT, PVCC, BTST, SW	Adapter present, V_{ACDET} > 2.4 V, charge disabled		100	200	µA
I_{AC}	Adapter quiescent current	V_{PVCC} = 20 V, charge disabled		1	1.5	mA
INTERNAL SOFT START (8 steps to regulation current)						
	Soft start steps			8		step
	Soft start time of each step (512 PWM cycles)			853		µs
LOGIC INPUT PIN CHARACTERISTICS (CE, TRICKLE)						
V_{IN_LO}	Input low threshold voltage				0.8	V
V_{IN_HI}	Input high threshold voltage		2.1			
$R_{PULLDOWN}$	PIN pull down resistance inside IC	V = 0 to V_{REGN}		1		MΩ
$T_{CE_ENCHARGE}$	Delay from CE=HIGH to charge enable (6)	F_s=300 kHz - 800 kHz		2		ms
LOGIC INPUT PIN CHARACTERISTICS (CELLS)						
V_{IN_LO}	Input low threshold voltage, 3 cells	CELLS voltage falling edge			0.5	V
V_{IN_FLOAT}	Input float threshold voltage, 2 cells	CELLS voltage rising for MIN, CELLS voltage falling for MAX	0.8		1.8	
V_{IN_HI}	Input high threshold voltage, 4 cells	CELLS voltage rising	2.5			
I_{BIAS_FLOAT}	Input bias float current for 2 cell selection	VCE = 0 to VREGN	–1		1	µA
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS ($\overline{\text{EXTPWR}}$, $\overline{\text{DPMDET}}$, $\overline{\text{LPMOD}}$)						
V_{OUT_LO}	Output low saturation voltage	Sink Current = 5 mA			0.5	V
	Leakage current	Pull up to 3.3 v			1	µA
	$\overline{\text{DPMDET}}$ delay, both edge			5		ms

(6) Verified by design

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TYPICAL CHARACTERISTICS

Table 2. Table of Graphs(1) F_s=400 kHz, Ta = 25 °C

Y	X	Figure
VREF Load and Line Regulation	vs Load Current	Figure 3
REGN Load and Line Regulation	vs Load Current	Figure 4
BAT Voltage	vs VADJ/VDAC Ratio	Figure 5
BAT Voltage Regulation Accuracy	vs Setpoint	Figure 6
Charge Current	vs ISET/VDAC Ratio	Figure 7
Charge Current Regulation Accuracy	vs V(CSP-CSN) Setpoint	Figure 8
Input Current	vs ACSET/VDAC Radio	Figure 9
DPM Accuracy	vs V(ACP-ACN) Setpoint	Figure 10
BAT Voltage Regulation Accuracy	vs Charge Current	Figure 11
V_IADAPT Accuracy	vs V(ACP-ACN) Voltage	Figure 12
Trickle Charge Current	vs BAT Voltage	Figure 13
DPM and Charge Current	vs System Current	Figure 14
REF, REGN, and $\overline{\text{EXTPWR}}$ Startup (CE=HIGH)		Figure 15
Transient System Load (DPM) Response Transition		Figure 16
Transient Response of IADAPT and $\overline{\text{LPMOD}}$		Figure 17
Battery Overcurrent Protection (OCP)		Figure 18
Battery to Ground Short Transition		Figure 19
Battery to Ground Short Protection		Figure 20
Charge Enable and Current Soft-Start		Figure 21
Charge Disable		Figure 22
Trickle Disable and Current Soft-Start		Figure 23
Synchronous to Non-synchronous Transition		Figure 24
Non-synchronous to Synchronous Transition		Figure 25
Continuous Conduction Mode Switching Waveforms		Figure 26
Near 100% Duty Cycle Bootstrap Recharge Pulse		Figure 27
Efficiency	vs Battery Charge Current	Figure 28
Switch Frequency	vs Setting Resistor	Figure 29

(1) Test results based on Figure 2 application schematic. V_{IN} = 20 V, V_{BAT} = 3-cell Li-Ion, I_{CHG} = 3 A, $I_{ADAPTER_LIMIT}$ = 4 A, T_A = 25°C, unless otherwise specified.

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VREF LOAD AND LINE REGULATION vs Load Current

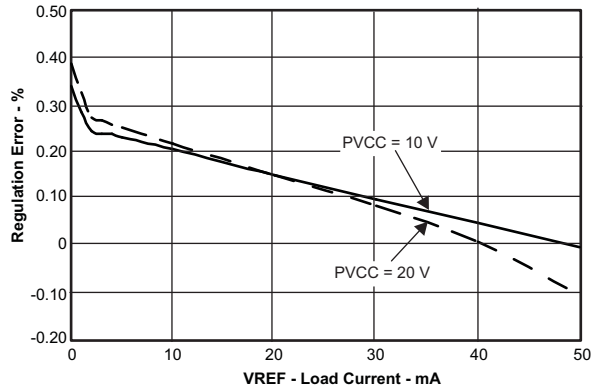


Figure 3.

REGN LOAD AND LINE REGULATION vs LOAD CURRENT

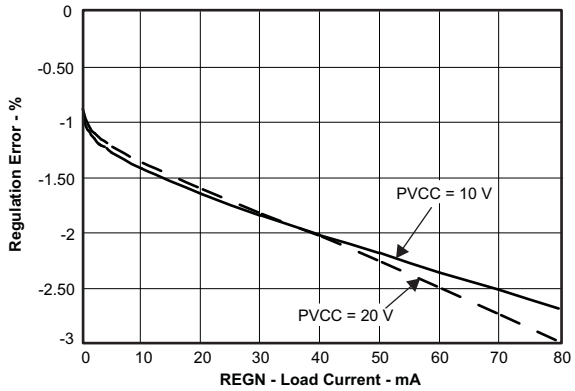


Figure 4.

BAT VOLTAGE vs VADJ/VDAC RATIO

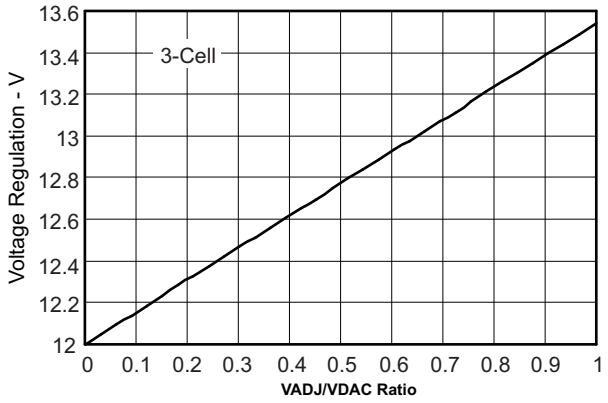


Figure 5.

BAT VOLTAGE REGULATION ACCURACY vs SETPOINT

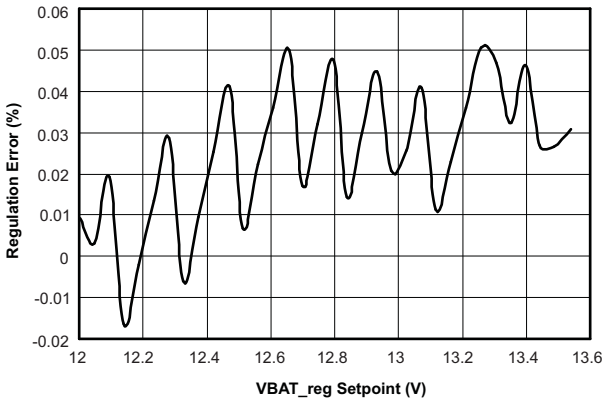


Figure 6.

CHARGE CURRENT vs ISET/VDAC

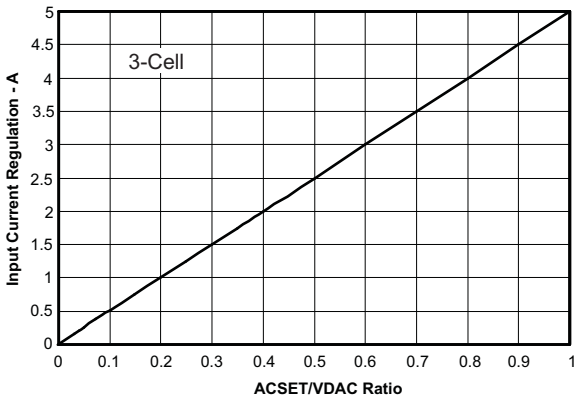


Figure 7.

CHARGE CURRENT REGULATION ACCURACY vs V(CSP-CSN) SETPOINT

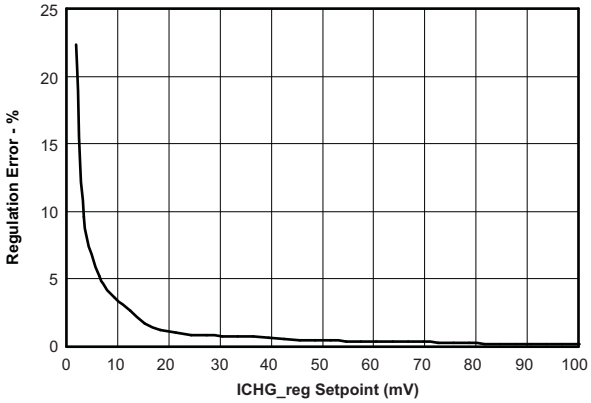


Figure 8.

INPUT CURRENT vs ACSET/VDAC RATIO

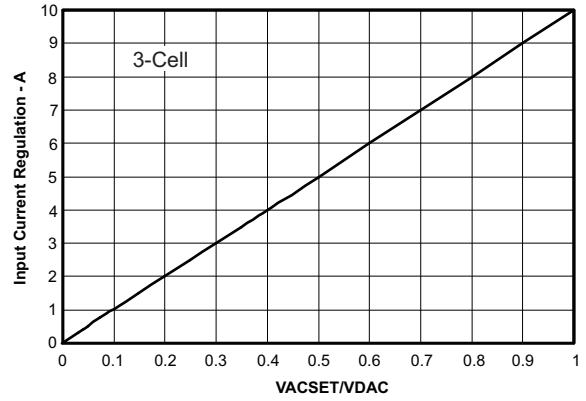


Figure 9.

DPM ACCURACY vs V(ACP-ACN) SETPOINT

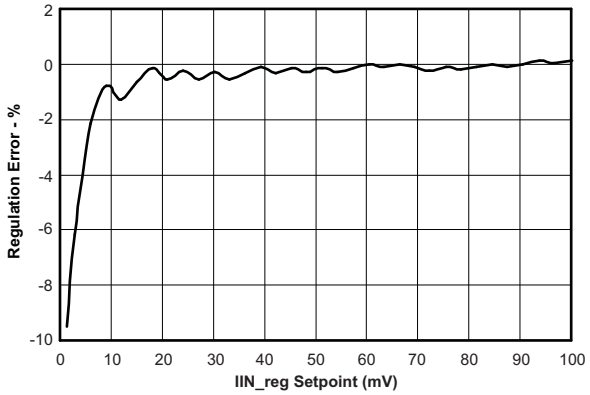


Figure 10.

BAT VOLTAGE REGULATION ACCURACY vs CHARGE CURRENT

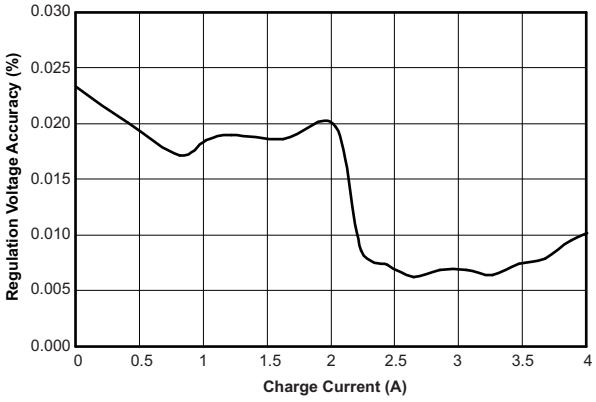


Figure 11.

V_IADAPT ACCURACY vs V(ACP-ACN) VOLTAGE

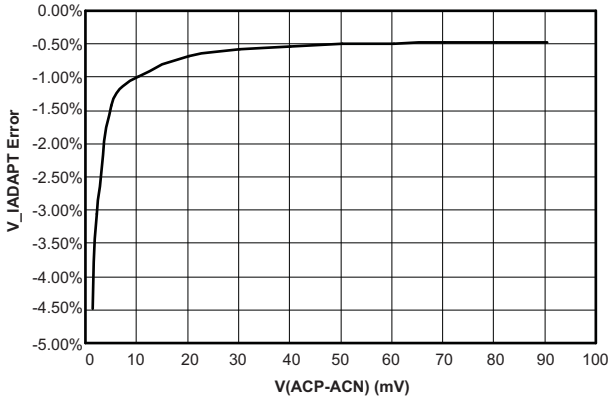


Figure 12.

TRICKLE CHARGE CURRENT vs BAT VOLTAGE

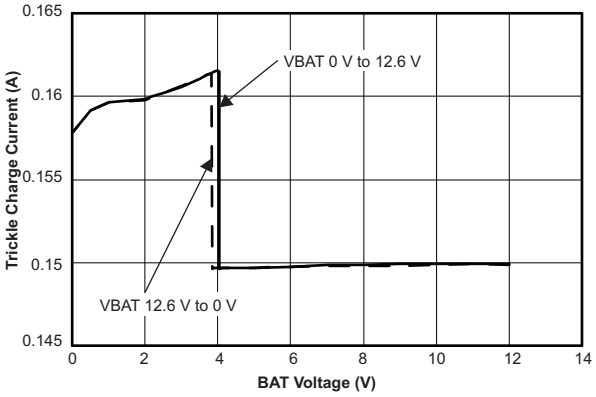


Figure 13.

DPM and CHARGE CURRENT vs SYSTEM CURRENT

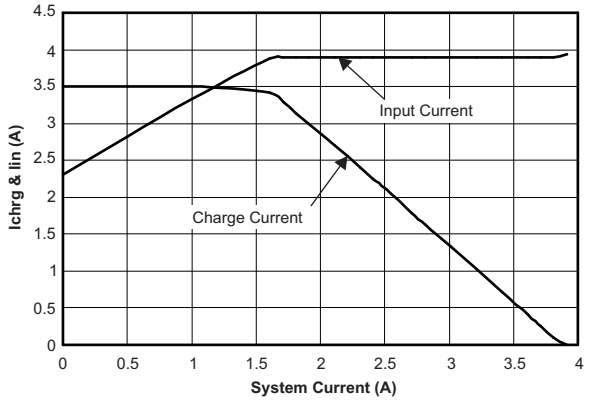


Figure 14.

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REF, REGN, and EXTPWR STARTUP (CE=HIGH)

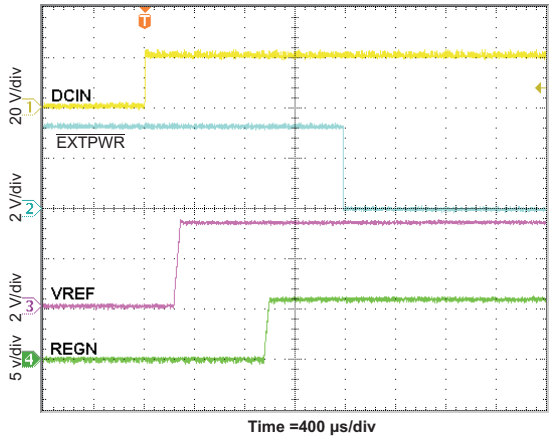


Figure 15.

TRANSIENT SYSTEM LOAD (DPM) RESPONSE TRANSITION

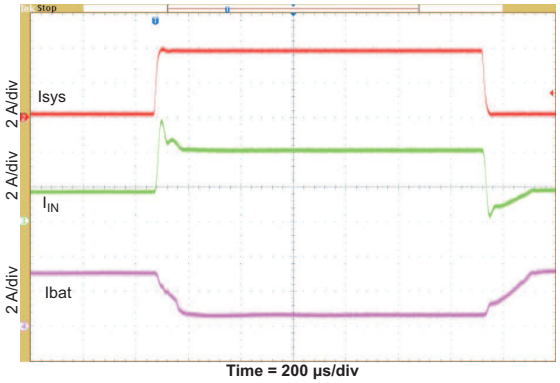


Figure 16.

TRANSIENT RESPONSE of IADAPT and LPMOD

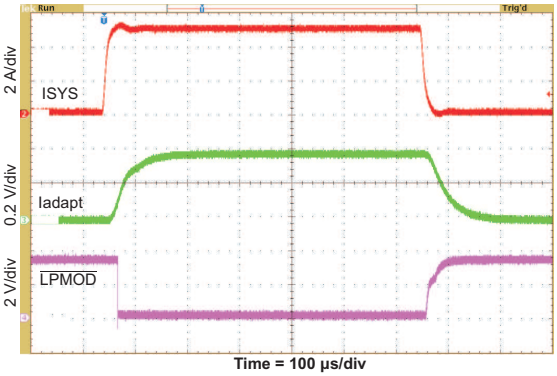


Figure 17.

BATTERY OVERCURRENT PROTECTION (OCP)

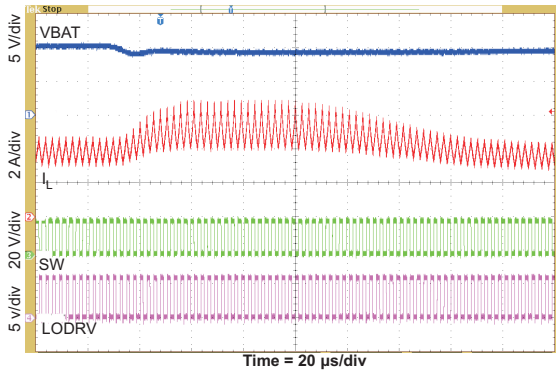


Figure 18.

BATTERY TO GROUND SHORT TRANSITION

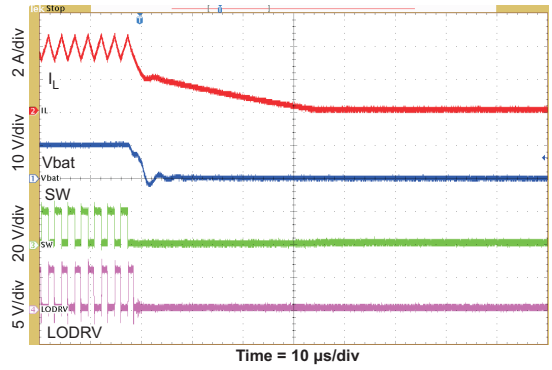


Figure 19.

BATTERY TO GROUND SHORT PROTECTION

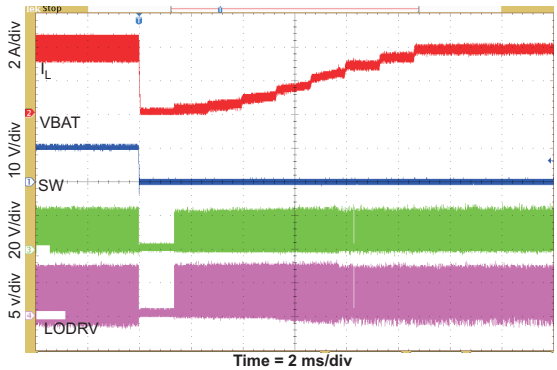


Figure 20.

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CHARGE ENABLE and CURRENT SOFT-START

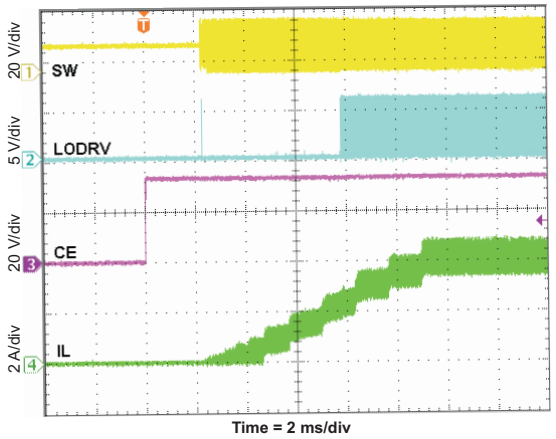


Figure 21.

CHARGE DISABLE

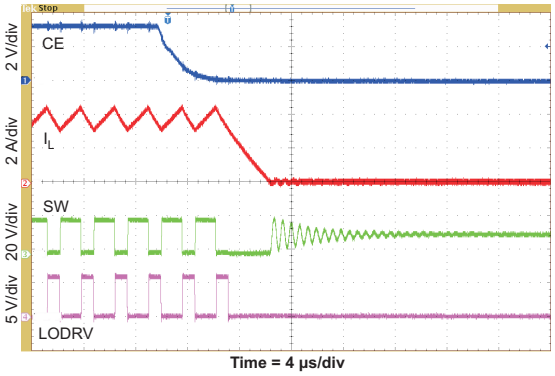


Figure 22.

TRICKLE DISABLE and CURRENT SOFT-START

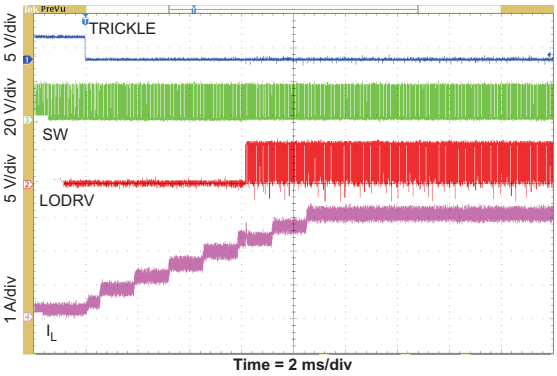


Figure 23.

SYNCHRONOUS to NON-SYNCHRONOUS TRANSITION

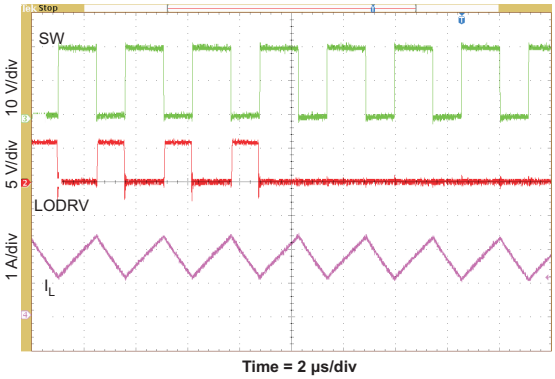


Figure 24.

NON-SYNCHRONOUS to SYNCHRONOUS TRANSITION

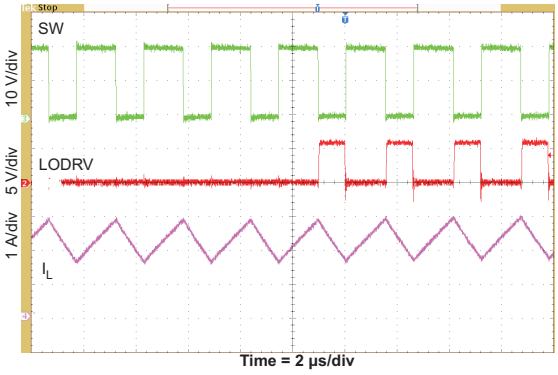


Figure 25.

CONTINUOUS CONDUCTION MODE SWITCHING WAVEFORMS

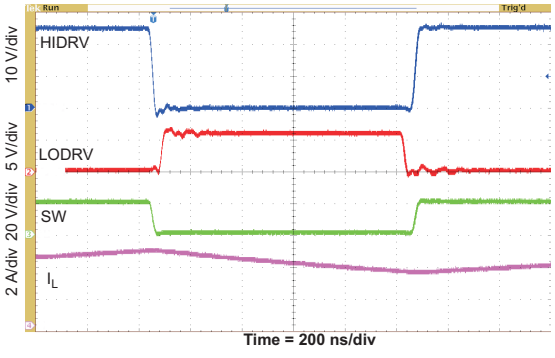


Figure 26.

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NEAR 100% DUTY CYCLE BOOTSTRAP RECHARGE PULSE

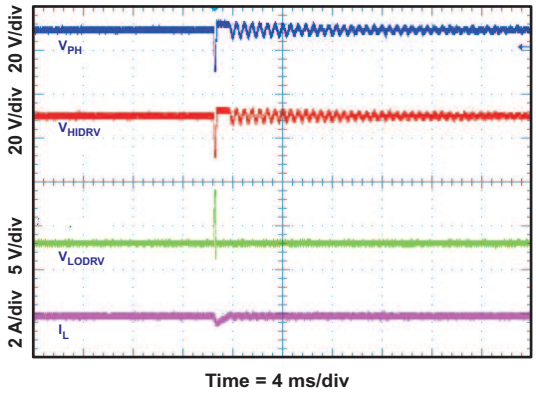


Figure 27.

EFFICIENCY vs BATTERY CHARGE CURRENT

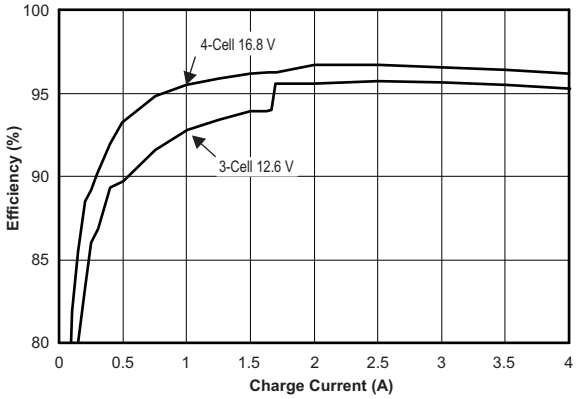


Figure 28.

SWITCH FREQUENCY vs SETTING RESISTOR

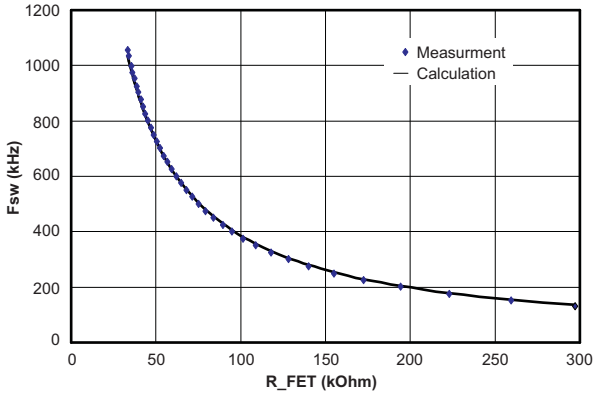
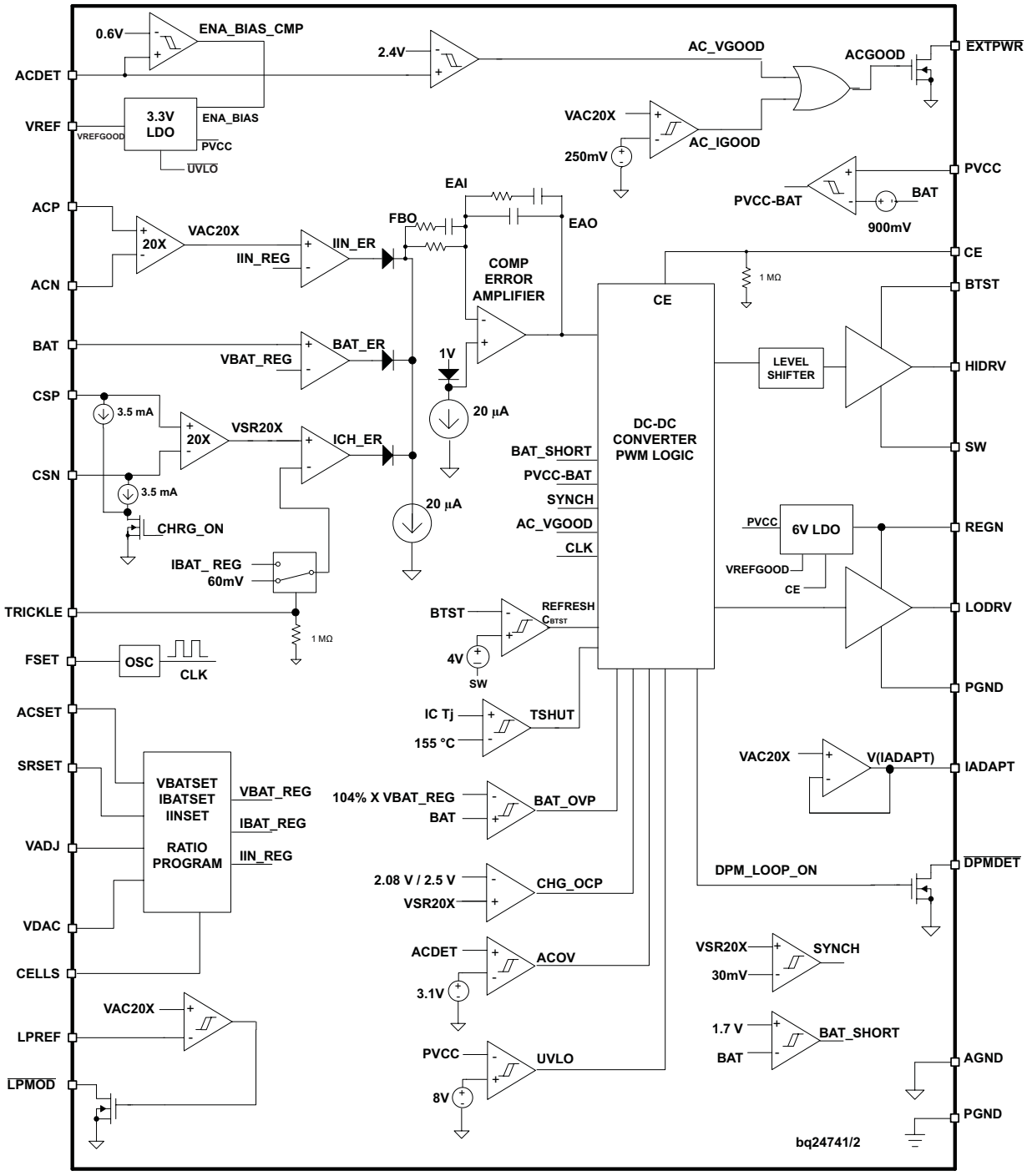


Figure 29.

FUNCTIONAL BLOCK DIAGRAM



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DETAILED DESCRIPTION

Converter Operation

The synchronous buck PWM converter uses a programmable-frequency (300 kHz to 800 kHz) voltage mode control scheme. A type III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected internally between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter should be selected to give a nominal resonant frequency within 8 kHz to 12.5 kHz to have good loop compensation.

Where resonant frequency, f_o, is give by:

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}} \quad (1)$$

Where L_o, C_o are the total output filter inductance and capacitance

An internal saw-tooth ramp is compared to the internal EAO error control signal to vary the duty-cycle of the converter. The ramp height is fixed 1.33 V. The ramp is offset by 300 mV in order to allow zero percent duty-cycle, when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate drive logic allows achieving 99.98% duty-cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to SW pin voltage falls below 4 V, then the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the SW node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BTST-SW) voltage is detected to fall low again due to leakage current discharging the BTST capacitor below the 4 V, and the reset pulse is reissued.

The oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region. The charge current sense resistor RSR should be placed with at least half or more of the total output capacitance placed before the sense resistor contacting both sense resistor and the output inductor; and the other half or remaining capacitance placed after the sense resistor. The output capacitance should be divided and placed onto both sides of the charge current sense resistor. A ratio of 50:50 percent gives the best performance; but the node in which the output inductor and sense resistor connect should have a minimum of 50% of the total capacitance. This capacitance provides sufficient filtering to remove the switching noise and give better current sense accuracy. The type III compensation provides Phase boost near the cross-over frequency, giving sufficient Phase margin.

Synchronous and Non-Synchronous Operation

The charger operates in non-synchronous mode when the sensed charge current is below the charge under-current comparator threshold (30 mV). Otherwise, the charger operates in synchronous mode. This part is designed for 20 mΩ charge current sense resistor and the SYNC/NON-SYNC threshold is 1.5 A. If 10 mΩ is used, the SYNC/NON-SYNC threshold will be 3 A.

During synchronous mode, the low-side n-channel power MOSFET is on, when the high-side n-channel power MOSFET is off. The internal gate drive logic ensures there is break-before-make switching to prevent shoot-through currents. During the 25 ns dead time where both FETs are off, the back-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn-on keeps the power dissipation low, and allows safely charging at high currents. During synchronous mode the inductor current is always flowing and operates in Continuous Conduction Mode (CCM), creating a fixed two-pole system.

During non-synchronous operation, the low side MOSFET will stay off during the off-time unless the voltage on the bootstrap capacitor drops below 4 V. If this occurs, the high side FET will be turned off and the 80ns low-side MOSFET recharge pulse will be initiated. The 80 ns pulse pulls the SW node (connection between high and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring. The inductor current is blocked by the off low-side MOSFET, and the inductor current will become discontinuous. This mode is called Discontinuous Conduction Mode (DCM).

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During the DCM mode the loop response automatically changes and has a single pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage. At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 80ns recharge pulse. The charge should be low enough to be absorbed by the input capacitance.

Whenever the converter goes into zero percent duty-cycle, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (no 80ns recharge pulse) either, and there is no discharge from the battery.

Battery Voltage Regulation

The bq24741/2 uses a high-accuracy voltage regulator for charging voltage. The regulation voltage is ratio-metric with respect to VDAC. The ratio of VADJ and VDAC provides extra 12.5% adjust range on V_{BATT} regulation voltage. By limiting the adjust range to 12.5% of the regulation voltage, the external resistor mismatch error is reduced from ±1% to ±0.1%. Therefore, an overall voltage accuracy as good as 0.5% is maintained, while using 1% mis-match resistors. Ratio-metric conversion also allows compatibility with D/As or microcontrollers (µC). The battery voltage is programmed through VADJ and VDAC using the following equation:

$$V_{BATT} = \text{cell count} \times \left[4\ V + \left(0.512 \times \frac{V_{VADJ}}{V_{VDAC}} \right) \right] \quad (2)$$

The input voltage range of VDAC is between 2.6V and 3.6V. VADJ is set between 0 and VDAC.

CELLS pin is the logic input for selecting cell count. Connect CELLS to charge 2, 3, or 4 Li+ cells. When charging other cell chemistries, use CELLS to select an output voltage range for the charger.

Table 3. Cell-Count Selection

CELLS	CELL COUNT
Float	2
AGND	3
VREF	4

The per-cell battery termination voltage is function of the battery chemistry. Consult the battery manufacturer to determine this voltage.

The BAT pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, or directly on the output capacitor. A 0.1µF ceramic capacitor from BAT to AGND is recommended to be as close to the BAT pin as possible to decouple high frequency noise.

Battery Current Regulation

The ISET input sets the maximum charging current. Battery current is sensed by resistor RSR connected between CSP and CSN. The full-scale differential voltage between CSP and CSN is 100 mV. Thus, for a 0.020 Ω sense resistor, the maximum charging current is 5 A. ISET is ratio-metric with respect to VDAC using the following equation:

$$I_{CHARGE} = \frac{V_{ISET}}{V_{VDAC}} \times \frac{0.10}{R_{SR}} \quad (3)$$

The input voltage range of ISET is between 0 and VDAC, up to 3.6 V.

The CSP and CSN pins are used to sense across R_{SR} with default value of 20 mΩ. However, resistors of other values can also be used. For a larger the sense resistor, you get a larger sense voltage, and a higher regulation accuracy; but, at the expense of higher conduction loss.

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Trickle Charge Current Regulation

The TRICKLE pin is provided to allow accurate current regulation at very low charge current. When CE is set to HIGH, a logic HIGH level is applied to the TRICKLE pin, the charger will regulate 3 mV from CSP to CSN (150 mA with a 20 mΩ sense resistor), regardless of the voltage applied to the ISET pin. When TRICKLE is LOW, ISET is used to program the charge current.

Input Adapter Current Regulation

The total input current from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the input current exceeds the input current limit set by ACSET. The current capacity of the AC adapter can be lowered, reducing system cost.

Similar to setting battery-regulation current, adapter current is sensed by resistor R_{AC} connected between ACP and ACN. Its maximum value is set by ACSET, which is ratiometric with respect to VDAC, using Equation 4.

$$I_{ADAPTER} = \frac{V_{ACSET}}{V_{VDAC}} \times \frac{0.10}{R_{AC}} \quad (4)$$

The input voltage range of ACSET is between 0 and V_{DAC}, up to 3.6 V.

The ACP and ACN pins are used to sense R_{AC} with a default value of 10 mΩ. However, resistors of other values can also be used. A larger sense-resistor value yields a larger sense voltage, and a higher regulation accuracy. However, this is at the expense of a higher conduction loss.

Adapter Detect and Power Up

An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The adapter detect threshold should typically be programmed to a value greater than the maximum battery voltage and lower than the minimum allowed adapter voltage. The ACDET divider should be placed before the ACFET in order to sense the true adapter input voltage whether the ACFET is on or off.

If ACDET is below 0.6 V but PVCC is above 8 V, part of the bias is enabled, including a crude bandgap reference, IADAPT is disabled and pulled down to GND. The total quiescent current is less than 10 μA.

Once ACDET rises above 0.6 V and PVCC is above 8 V, all the bias circuits are enabled and VREF goes to 3.3 V; and REGN output goes to 6 V if CE is HIGH. IADAPT becomes valid to proportionally reflect the adapter current.

When ACDET keeps rising and passes 2.4 V, a valid AC adapter is present. 8 ms later, charge is allowed to turn on.

Programming the PWM Switching Frequency

To program the PWM switching frequency, place a resistor from the FSET pin to ground, according to the following formula:

$$R_{FSET} = \frac{41 \times 10^3}{F_s} - 6.25 \ (k\Omega) \quad (5)$$

Where R_{FSET} (kΩ) is the resistor from the FSET pin to ground, and F_s (kHz) is the desired switching frequency. The switching frequency should be programmed between 300 kHz and 800 kHz.

Enable and Disable Charging

The following conditions must be valid before the charge function is enabled:

- CE is HIGH
- Adapter is detected
- Adapter voltage is higher than PVCC-BAT threshold
- Adapter is not over voltage
- The VREF and REGEN regulators are above 90% of the final values

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- Thermal Shut (TSHUT) is not active
- The PWM frequency is programmed inside the allowable range

There's a 2ms charge enable delay from when adapter is detected to when the charger is allowed to turn on.

One of the following conditions will stop on-going charging:

- CE is LOW
- Adapter is removed
- Adapter Voltage is lower than PVCC-BAT threshold
- Adapter is over voltage
- Adapter is over current
- TSHUT IC temperature threshold is reached (155 °C on rising-edge with 20 °C hysteresis).

Automatic Internal Soft-Start Charger Current

The charger automatically soft-starts the charger regulation current every time the charger is enabled to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts around 1ms, for a typical rise time of 8ms. No external components are needed for this function.

High Accuracy IADAPT Using Current Sense Amplifier (CSA)

An industry standard, high accuracy current sense amplifier (CSA) is used to monitor the input current by the host or some discrete logic through the analog voltage output of the IADAPT pin. The CSA amplifies the input sensed voltage of ACP–ACN by 20x through the IADAPT pin. The IADAPT output is a voltage source 20 times the input differential voltage. Once PVCC is above 8 V and ACDET is above 0.6 V, IADAPT no longer stays at ground, but becomes active. If the user wants to lower the voltage, they could use a resistor divider from IOUT to AGND, and still achieve accuracy over temperature as the resistors can be matched their thermal coefficients.

Input Overvoltage Protection (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. Once the adapter voltage is 30% above adapter detect voltage, (ACDET pin voltage is 30% above 2.4 V (2.4 V X 130% = 3.1 V), charge is disabled. ACOV does not latch, and normal operation resumes when ACDET < 3.1 V.

Input Undervoltage Lock Out (UVLO)

The system must have a typical 8 V PVCC voltage to allow proper operation. This PVCC voltage could come from an input adapter . When the PVCC voltage is below 8 V the bias circuits REGN and VREF stay inactive, even with ACDET above 0.6 V.

Battery Overvoltage Protection

The converter will not allow the high-side FET to turn-on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected.

Charge Overcurrent Protection

The charger has a secondary over-current protection. It monitors the charge current, and prevents the current from exceeding 6.25A peak value with a 20 mΩ sensing resistor. The high-side gate drive turns off when the over-current is detected, and automatically resumes at the next switching cycle that occurs after the current falls below the OCP threshold. When the BAT-GND short is detected, the charger will be automatically shut down immediately and then restarts again 100 µs later.

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Short-Circuit Protection

The charger has a secondary short-circuit protection. It monitors the voltage-drop (detect ACP-SW for protecting high-side MOSFET and detect SW-AGND for protecting low-side MOSFET) to prevents the short-circuit current from exceeding a certain value to damage the charger. It will be monitored after typical blanking time of 100ns. The MOSFET gate driver signal turns off when the short-circuit current is detected in every switching cycle. The charger will shut-down and latch off after this occurs 7 times. POR or toggling CE pin can resume normal charge function.

Thermal Shutdown Protection

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 155 °C. The charger stays off until the junction temperature falls below 135 °C, then the charger will soft-start again if all other enable charge conditions are valid.

Input Low Power Detection

In order to optimize the system performance, the HOST keeps an eye on the adapter current. Once the adapter current is above a threshold set via LPREF, the $\overline{\text{LPMOD}}$ pin sends a signal to the HOST. The signal alarms the host that input power has exceeded the programmed limit. The $\overline{\text{LPMOD}}$ pin is an open-drain output. Connect a pull-up resistor to $\overline{\text{LPMOD}}$. The $\overline{\text{LPMOD}}$ output is logic LOW when the 20X current sense voltage (20 x $V_{(ACP-ACN)}$) is higher than the LPREF input voltage. The LPREF threshold may be set by an external resistor divider using VREF, or may be programmed from a resistor divider off of ACSET to maintain an LPREF voltage proportional to the adapter current. The $\overline{\text{LPMOD}}$ comparator has an internal 6% hysteresis built in.

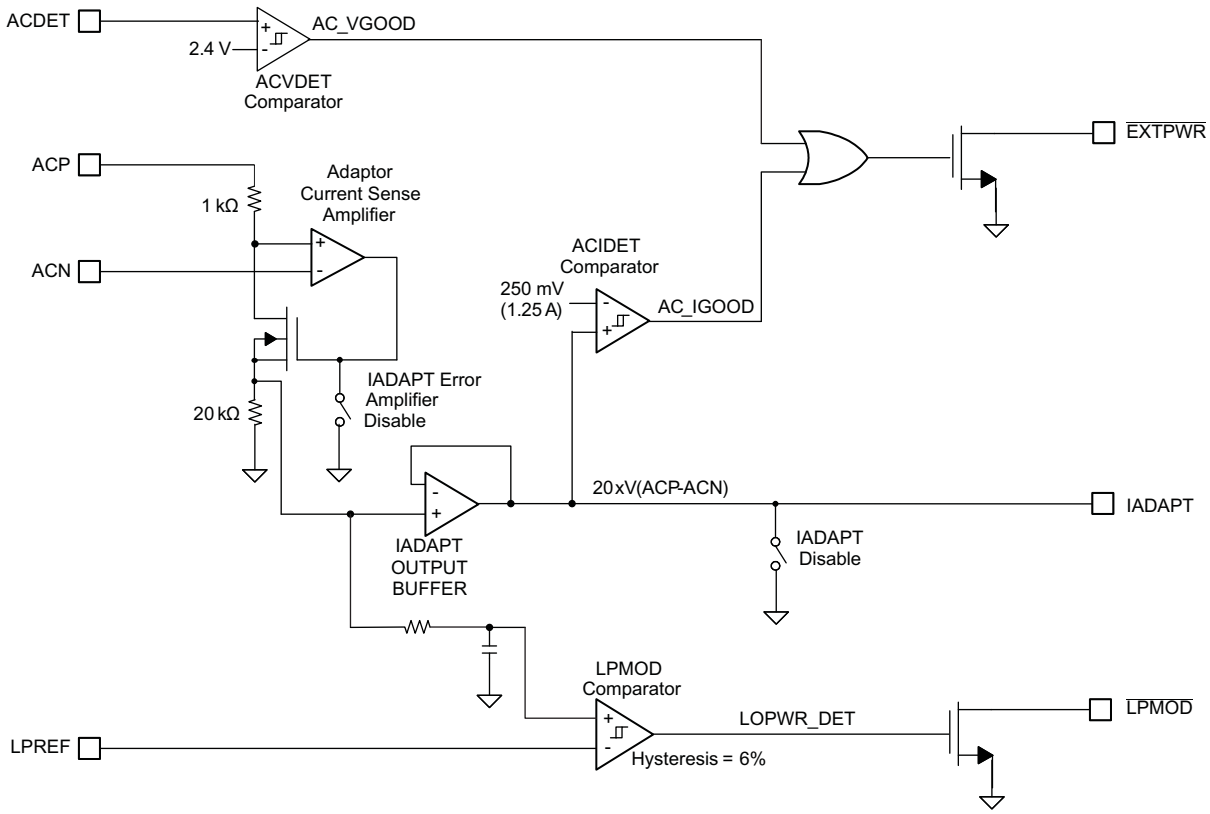


Figure 30. $\overline{\text{EXTPWR}}$, LPREF, and $\overline{\text{LPMOD}}$ Logic

Status Outputs ($\overline{\text{EXTPWR}}$, $\overline{\text{LPMOD}}$, $\overline{\text{DPMDET}}$ Pin)

Three status outputs are available, and they all require external pull up resistors to pull the pins to system digital rail for a high level.

$\overline{\text{EXTPWR}}$ open-drain output goes low under each of the three conditions:

1. ACDET is above 2.4 V
2. Adapter current is above 1.25 A using a 10mohm sense resistor (IADAPT voltage above 250 mV)

Internally, the AC current detect comparator looks between the output of the 20x adapter current amplifier and an internal 250mV threshold. $\overline{\text{EXTPWR}}$ indicates a good adapter is connected because of valid voltage or current.

$\overline{\text{LPMOD}}$ output goes low when the input current is higher than the programmed threshold via LPREF pin. Hysteresis is internally set to 6% of the programmed $\overline{\text{LPMOD}}$ threshold.

$\overline{\text{DPMDET}}$ open-drain output goes low when the DPM loop is active to reduce the battery charge current.

Table 4. Component List for Typical System Circuit of Figure 1

PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2, Q3	3	P-channel MOSFET, -30V,-6A, SO-8, Vishay-Siliconix, Si4435
Q4	1	N-channel Dual-MOSFET, 30V, 7.5A, SO-8, Fairchild, FDS8978
D1, D2	2	Diode, Dual Schottky, 30V, 200mA, SOT23, Fairchild, BAT54C
R_{AC}	1	Sense Resistor, 10mΩ, 1%, 1W, 2010, Vishay-Dale, WSL2010R0100F
R_{SR}	1	Sense Resistor, 20mΩ, 1%, 1W, 2010, Vishay-Dale, WSL2010R0200F
L1	1	Inductor, 10µH, 24.8mΩ Vishay-Dale, IHLP5050CE-01
C1	1	Capacitor, Ceramic, 2.2µF, 35V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E225M
C6, C7, C11, C12	4	Capacitor, Ceramic, 10µF, 35V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E106M
C4, C10	2	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 2012, TDK, C2012X7R1E105K
C13	1	Capacitor, Ceramic, 100nF, 25V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
C2, C3, C8, C9, C13, C14, C15, C16	6	Capacitor, Ceramic, 0.1µF, 50V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
C5	1	Capacitor, Ceramic, 100pF, 25V, 10%, X7R, 0805, Kemet, C0805C101K5RACTU
R1	1	Resistor, Chip, 464kΩ, 1/16W, 1%, 0402
R2	1	Resistor, Chip, 66.5kΩ, 1/16W, 1%, 0402
R3, R4, R5, R15	4	Resistor, Chip, 10kΩ, 1/16W, 5%, 0402
R6	1	Resistor, Chip, 97.6kΩ, 1/16W, 1%, 0402
R7	1	Resistor, Chip, 73.2kΩ, 1/16W, 1%, 0402
R8	1	Resistor, Chip, 26.7kΩ, 1/16W, 1%, 0402
R9	1	Resistor, Chip, 60.4kΩ, 1/16W, 1%, 0402
R10	1	Resistor, Chip, 40.2kΩ, 1/16W, 1%, 0402
R11	1	Resistor, Chip, 2Ω, 1W, 5%, 2012
R12	1	Resistor, Chip, 102kΩ, 1/16W, 1%, 0402
R13	1	Resistor, Chip, 64.9kΩ, 1/16W, 1%, 0402
R14	1	Resistor, Chip, 120kΩ, 1/16W, 1%, 0402

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APPLICATION INFORMATION

Inductor Selection

The bq24741/2 can program the switching frequency between 300k and 800kHz for different applications. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (6)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D=V_{OUT}/V_{IN}$), switching frequency (f_s) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (7)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9V to 12.6V for 3-cell battery pack. For 20V adapter voltage, 10V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12V to 16.8V, and 12V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

The bq24741/2 has charge under current protection (UCP) by monitoring charging current sensing resistor. The Typical UCP threshold is 30mV falling edge and 40mV rising edge corresponding to 1.5A falling edge and 2A rising edge for a 20mΩ charging current sensing resistor. To prevent negative inductor current, the inductance must be high enough so that peak to peak ripple current is less than 3A (for a 20mΩ charging current sensing resistor) when charging current tapers down. Considering UCP threshold tolerance for worst case, peak to peak ripple current less than 2.5A for a 20mΩ charging current sensing resistor is preferred.

Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (8)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for 19-20V input voltage. 10-20µF capacitance is suggested for typical of 3-4A charging current.

Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (9)$$

The bq24741/2 has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 8 kHz and 12.5 kHz.

The preferred ceramic capacitor is 25V, X7R or X5R for output capacitor. 10-20µF capacitance is suggested for practical application. Two capacitors, one capacitor is located before and another one after charging current sensing resistor to get the best average charge current regulation accuracy.

Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 5.9V of gate drive voltage. 30V or higher voltage rating MOSFETs are preferred for 19-20V input voltage.

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Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD} \qquad FOM_{bottom} = R_{DS(on)} \times Q_G \tag{10}$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ®$_{DS(ON)}$), input voltage (V_{IN}), switching frequency (F), turn on time (t_{on}) and turn off time (t_{toff}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times \left(t_{on} + t_{off}\right) \times f_S \tag{11}$$

The first item represents the conduction loss. Usually MOSFET RDS(ON) increases by 50% with 100ºC junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \; t_{off} = \frac{Q_{SW}}{I_{off}} \tag{12}$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and Ioff is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \tag{13}$$

Gate driving current total can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (Ron) and turn-off gate resistance ®$_{off}$) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \; I_{off} = \frac{V_{plt}}{R_{off}} \tag{14}$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \tag{15}$$

When charger operates in non-synchronous mode, the bottom-side MOSFET is off. As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The body diode power loss depends on its forward voltage drop (V_F), non-synchronous mode charging current ($I_{NONSYNC}$), and duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D) \tag{16}$$

The maximum charging current in non-synchronous mode can be up to 2.25A for a 20mΩ charging current sensing resistor considering IC UCP threshold tolerance. The minimum duty cycle happens at lowest battery voltage. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at PVCC pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent over voltage event on PVCC pin.

There are several methods to damping or limit the over voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over voltage level to an IC safe level. However these two solutions may not have low cost or small size.

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A cost effective and small size solution is shown in Figure 31. The R1 and C1 is composed of a damping RC network to damp the hot plug-in oscillation. As a result the over voltage spike is limited to a safe level. D1 is used for reverse voltage protection for PVCC pin. C2 is PVCC pin decoupling capacitor and it should be place to PVCC pin as close as possible. C2 value should be much less than C1 value so R1 can dominant the equivalent ESR value to get enough damping effect. R2 is used to limit inrush current of D1 to prevent D1 getting damage when adapter hot plug-in. R1 has high inrush current. R1 package must be sized enough to handle inrush current power loss according to resistor manufacturer's datasheet. The filter components value always need to be verified with real application and minor adjustments may need to fit in the real application circuit.

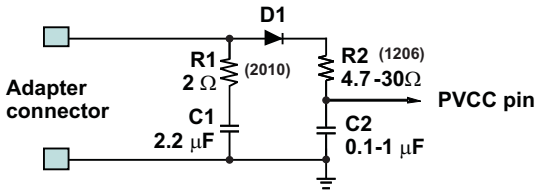


Figure 31. Input Filter

bq24741/2 Design Guideline

The bq24741/2 has a unique short circuit protection feature. Its cycle-by-cycle current monitoring feature is achieved through monitoring the voltage drop across Rdson of the MOSFETs after a certain amount of blanking time. In case of MOSFET short or inductor short circuit, the over current condition is sensed by two comparators and two counters will be triggered. After seven times of short circuit events, the charger will be latched off. The way to reset the charger from latch-off status is to toggle the CE pin or IC power on reset. Figure 32 shows the bq24741/2 short circuit protection block diagram.

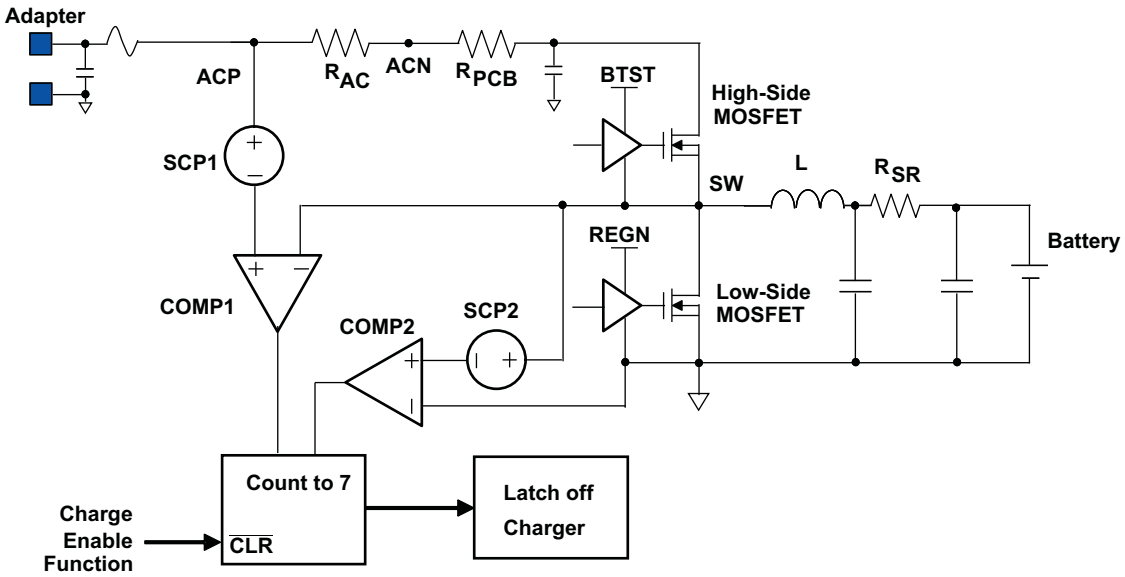


Figure 32. Block Diagram of bq24741/2 Short Circuit Protection

In normal operation, low side MOSFET current is from source to drain which generates negative voltage drop when it turns on, as a result the over current comparator can not be triggered. When high side switch short circuit or inductor short circuit happens, the large current of low side MOSFET is from drain to source and can trig low side switch over current comparator. the bq24741/2 senses low side switch voltage drop by SW pin and AGND pin.

The high-side FET short is detected by monitoring the voltage drop between ACP and SW. As a result, it not only monitors the high side switch voltage drop, but also the adapter sensing resistor voltage drop and PCB trace voltage drop from ACN terminal of R_{AC} to charger high side switch drain. Usually, there is a long trance between input sensing resistor and charger converting input, a careful layout will minimize the trace effect.

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To prevent unintentional charger shut down in normal operation, MOSFET $R_{DS(on)}$ selection and PCB layout is very important. Figure 33 shows a need improve PCB layout example and its equivalent circuit. In this layout, system current path and charger input current path is not separated, as a result, the system current causes voltage drop in the PCB copper and is sensed by IC. The worst layout is when a system current pull point is after charger input; as a result all system current voltage drops are counted into over current protection comparator. The worst case for IC is the total system current and charger input current sum equals DPM current. When system pull more current, the charger IC tries to regulate R_{AC} current as a constant current by reducing charging current.

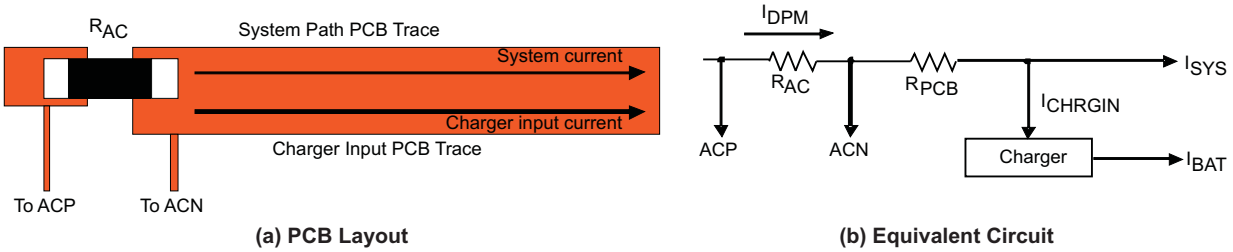


Figure 33. Need Improve PCB Layout Example

Figure 34 shows the optimized PCB layout example. The system current path and charge input current path is separated, as a result the IC only senses charger input current caused PCB voltage drop and minimized the possibility of unintentional charger shut down in normal operation. This also makes PCB layout easier for high system current application.

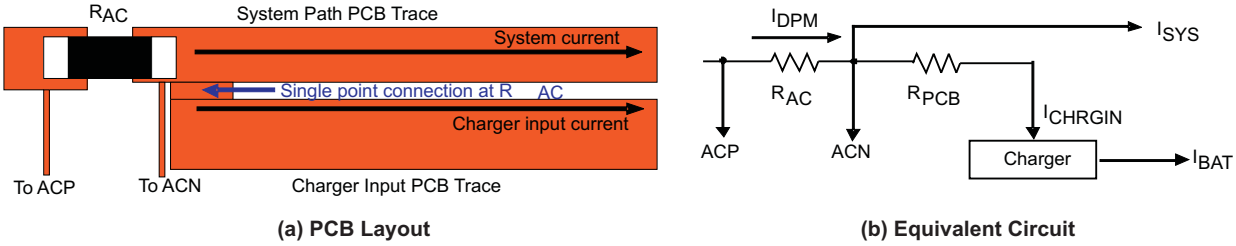


Figure 34. Optimized PCB Layout Example

The total voltage drop sensed by IC can be express as the following equation.

$$V_{top} = R_{AC} \times I_{DPM} + R_{PCB} \times \left(I_{CHRGIN} + \left(I_{DPM} - I_{CHRGIN}\right) \times k\right) + R_{DS(on)} \times I_{PEAK} \quad (17)$$

where the R_{AC} is the AC adapter current sensing resistance, I_{DPM} is the DPM current set point, R_{PCB} is the PCB trace equivalent resistance, I_{CHRGIN} is the charger input current, k is the PCB factor, $R_{DS(on)}$ is the high side MOSFET turn on resistance and I_{PEAK} is the peak current of inductor. Here the PCB factor k equals 0 means the best layout shown in Figure 34 where the PCB trace only goes through charger input current while k equals 1 means the worst layout shown in Figure 33 where the PCB trace goes through all the DPM current. The total voltage drop must below the high side short circuit protection threshold to prevent unintentional charger shut down in normal operation.

PCB Layout

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 35) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to switching MOSFET's supply and ground connections and use shortest copper trace connection. These parts should be placed on the same layer of PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET's gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of switching

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MOSFETs.

3. Place inductor input terminal to switching MOSFET's output terminal as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 36 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC.
5. Place output capacitor next to the sensing resistor output and ground.
6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
8. Route analog ground separately from power ground. Connect analog ground to AGND and connect power ground to PGND separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground (power pad should tie to analog ground in this case).
9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
10. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
11. The via size and number should be enough for a given current path.

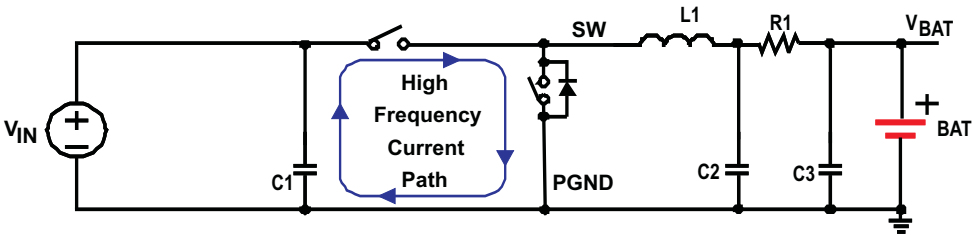


Figure 35. High Frequency Current Path

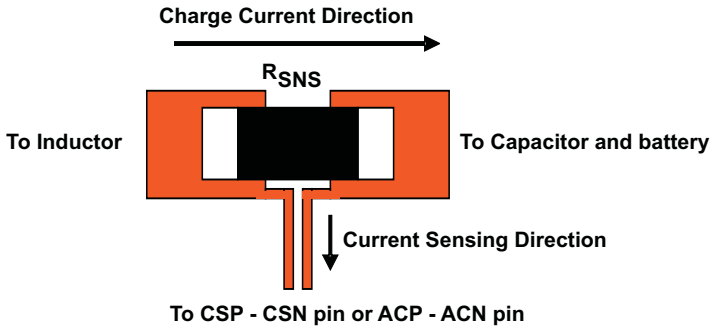


Figure 36. Sensing Resistor PCB Layout

Refer to the EVM design (SLUU284) for the recommended component placement with trace and via locations.

For the QFN information, refer to SCBA017 and SLUA271.

REVISION HISTORY

Changes from Revision A (March 2009) to Revision B **Page**

- Changed 8 V to 9 V 1
- Changed "Cells pin support two to for Li-Ion cells up to 18 V battery voltage" to Support two to four cells 1
- Added "FET/Inductor/Battery Short Protection" 1
- Added "Loop Compensation" 1
- Deleted "Internal Loop Compensation" bullet 1
- Added "Quiescent Current" 1
- Added 10Ω R16 to top of schematic 2
- Added 10Ω R16 to top of schematic 3
- Changed bq24742RHDR to bq24742RHDT 3
- Changed 8.0 V to 9.0 V in condition values 6
- Changed min voltage from 8 to 9 for V_{PVCC_OP} parameter 6
- Deleted VBAT_OP parameter from this section 6
- Changed 8.0 V to 9.0 V in condition values 7
- Changed 8.0 V to 9.0 V in condition values 8
- Changed "Short Circuit" to "MOSFET short" 8
- Changed VLS max value from 280 to 320 8
- Changed all instances of V_{PH} to V_{SW} in following section 8
- Changed 8.0 V to 9.0 V in condition values 9
- Deleted VCC pin 9
- Added graph: "Near 100% Duty Cycle.." 15
- Changed polarity of IIN_ER, BAT_ER, and ICH_ER op amps 16
- Added text note under equation 17
- Changed 8ms to 2ms 20
- Changed "This PVCC voltage could come from either input adapter or battery, using a diode-OR input." 20
- Added then the charger will soft-start again if all other enable change conditions are valid. 21
- Added added text, equations and illustrations from Inductor Selection to PCB Layout 23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24741RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24741RHDT	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24742RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24742RHDT	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

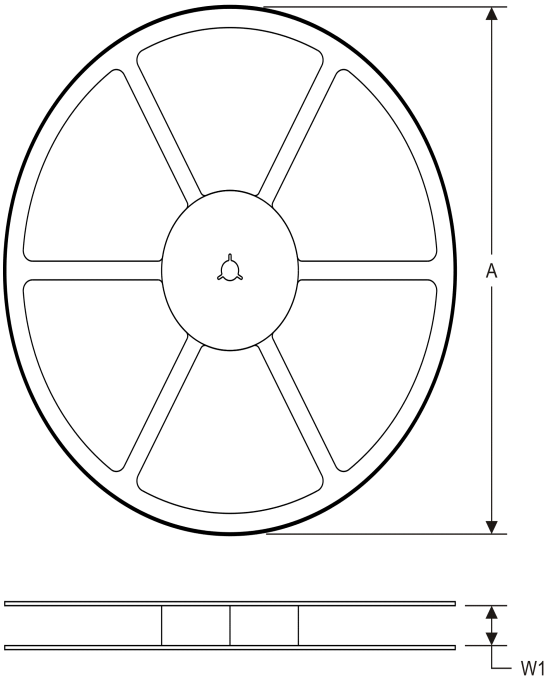
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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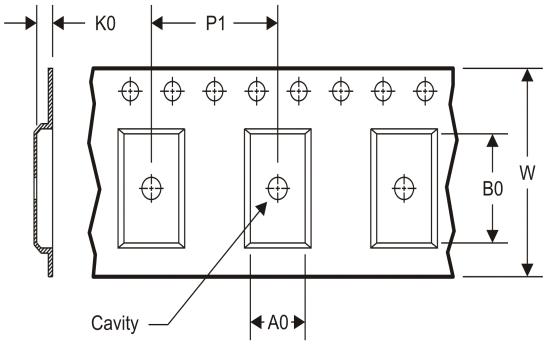
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



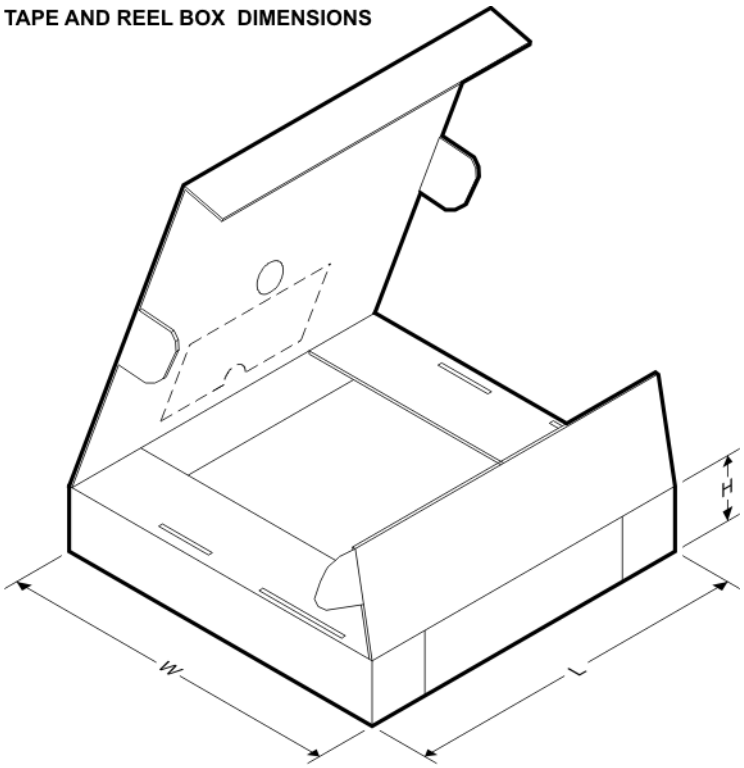
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24741RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24741RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24741RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24741RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24742RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24742RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24742RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24742RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

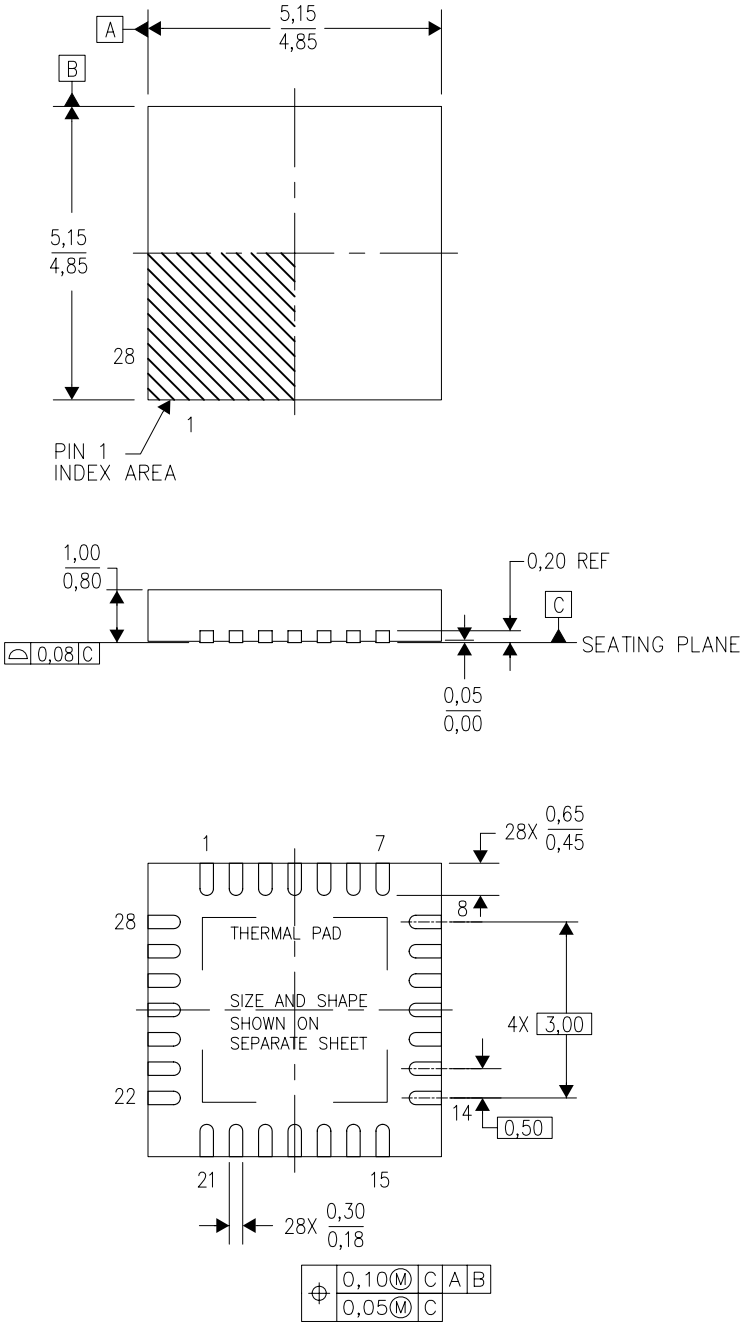
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24741RHDR	VQFN	RHD	28	3000	346.0	346.0	29.0
BQ24741RHDR	VQFN	RHD	28	3000	346.0	346.0	29.0
BQ24741RHDT	VQFN	RHD	28	250	210.0	185.0	35.0
BQ24741RHDT	VQFN	RHD	28	250	210.0	185.0	35.0
BQ24742RHDR	VQFN	RHD	28	3000	346.0	346.0	29.0
BQ24742RHDR	VQFN	RHD	28	3000	346.0	346.0	29.0
BQ24742RHDT	VQFN	RHD	28	250	210.0	185.0	35.0
BQ24742RHDT	VQFN	RHD	28	250	210.0	185.0	35.0

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



4204400/F 09/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

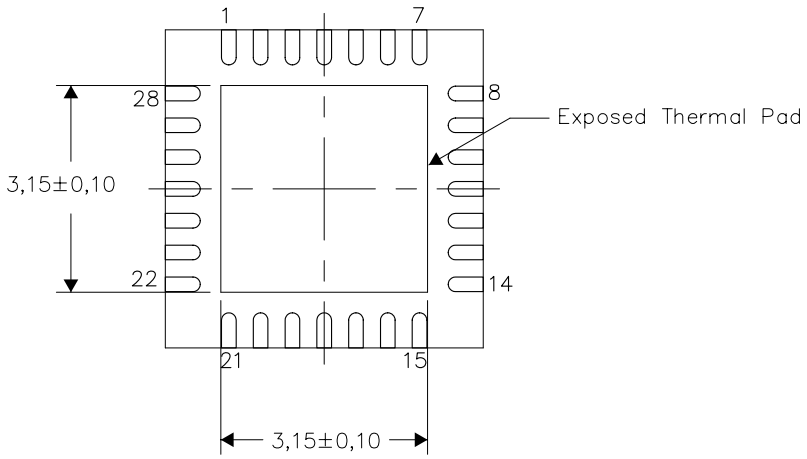
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



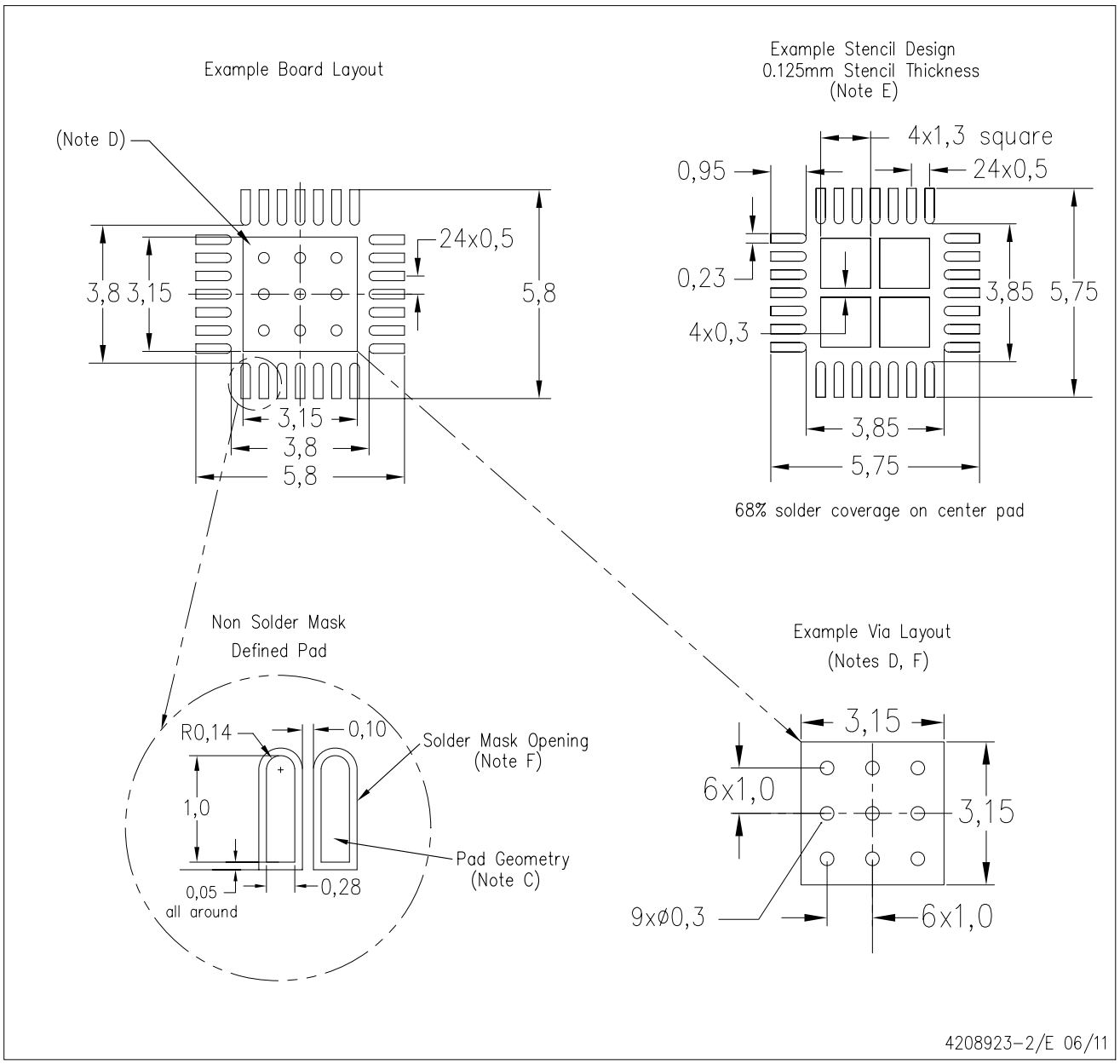
Bottom View

Exposed Thermal Pad Dimensions

4206358–2/I 05/11

NOTE: All linear dimensions are in millimeters

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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